# AMD RX881 Databook

**Technical Reference Manual**
**Rev 1.40**

P/N: 46136_rx881_ds_pub_1.40

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# Chapter 1
# Overview

## 1.1 Introducing the RX881

The RX881 is the latest system logic from AMD that supports AMD S1g3-socket CPUs, such as the Caspian-series processors.

The RX881 is pin-compatible with AMD's other mainstream 700 and 800-series products including the RS880, RS880M, RS780, RS780D, RS780M, RX780, RD780, and RX781, allowing a single design to target multiple market segments.

**Robust and Flexible Core Logic Features**

The RX881 supports a high speed HyperTransport™ interface to the AMD processor, running at a data rate of up to 4.4 GT/s and supporting both HT 1.0 and HT 3.0 protocols. The RX881 is ideally suited for 64-bit operating systems, and supports platform configurations with greater than 4GB of system memory. The rich PCI Express® (PCIe®) expansion capabilities of RX881 include support for PCI Express graphics and up to six other PCI Express peripherals, all supporting the PCI Express 2.0 standard with data rates of up to 5.0GT/s. These capabilities are complemented by the advanced I/O features of AMD's SB700 and SB800-series Southbridges.

**Low Power Consumption and Industry Leading Power Management**

The RX881 is manufactured using the power efficient 55 nm technology, and it supports a whole range of industry standards and power management features. It provides comprehensive support for the ACPI specification and AMD power management features such as AMD PowerNow!™.

## 1.2 RX881 Features

### 1.2.1 CPU HyperTransport™ Interface

- Supports 16-bit up/down HyperTransport (HT) 3.0 interface up to 4.4 GT/s.
- Supports 200, 400, 600, 800, and 1000 MHz HT1 frequencies.
- Supports 1.6, 1.8, 2.0, and 2.2 GHz HT3 frequencies.
- Supports AMD's S1g3-socket CPUs, including the Caspian-series processors.
- Supports LDTSTOP interface and CPU link stutter mode.

### 1.2.2 PCI Express® Interface

- Supports PCIe Gen2 (version 2.0).
- Optimized peer-to-peer and general purpose link performance.
- Highly flexible PCI Express implementation to suit a variety of platform needs.
- Supports a x16 graphics interface.
- Supports programmable lane reversal for the graphics link to ease motherboard layout when the end device does not support lane reversal.
- Supports six general purpose lanes, for up to six devices on specific ports. Possible configurations are listed in *Table 1-1*.

**Table 1-1 Possible Configurations for the PCIe® General Purpose Links**

| | Config. B | Config. C | Config. C2 | Config. E | Config. K | Config. L |
|---|---|---|---|---|---|---|
| GPP1 | x4 | x4 | x2 | x2 | x2 | x1 |
| GPP2 | - | - | - | - | - | x1 |
| GPP3 | - | - | x2 | x1 | x2 | x1 |
| GPP4 | - | - | - | x1 | - | x1 |
| GPP5 | x2 | x1 | x2 | x1 | x1 | x1 |
| GPP6 | - | x1 | - | x1 | x1 | x1 |

- Supports x1, x2, x4, x8, x12 and x16 polarity inversion.

### 1.2.3 A-Link Express II Interface

- One x4 A-Link Express II interface for connection to an AMD Southbridge. The A-Link Express II is a proprietary interface developed by AMD basing on the PCI Express technology, with additional Northbridge-Southbridge messaging functionalities.
- Supports programmable lane reversal to ease motherboard layout.

### 1.2.4 System Clocks

- Support for an external clock chip to generate PCIe and A-Link Express II clocks. Alternatively, internal generation for these clocks, with clock input from an SB800-series Southbridge, can be used (subject to characterization with actual RX881 and SB800-series devices).

### 1.2.5 Power Management Features

- Single chip solution in 55nm, 1.1V CMOS technology.
- Full ACPI 2.0 and IAPC (Instantly Available PC) power management support.
- The Chip Power Management Support logic supports four device power states defined for the OnNow Architecture—On, Standby, Suspend, and Off. Each power state can be achieved by software control bits.
- Hardware controlled intelligent clock gating enables clocks only to active functional blocks, and is completely transparent to software.
- Support for Cool'n'Quiet™ via FID/VID change.
- Support for AMD PowerNow!™.
- Clocks to every major functional block are controlled by a unique dynamic clock switching technique that is completely transparent to the software. By turning off the clock to the block that is idle or not used at that point, the power consumption can be significantly reduced during normal operation.
- Supports dynamic lane reduction for the PCIe graphics interface when coupled with an AMD-based graphics device, adjusting lane width according to required bandwidth.

### 1.2.6 PC Design Guide Compliance

The RX881 complies with all relevant Windows Logo Program (WLP) requirements from Microsoft for WHQL certification.

### 1.2.7 Test Capability Features

The RX881 has a variety of test modes and capabilities that provide a very high fault coverage and low DPM (Defect Per Million) ratio:

- Full scan implementation on the digital core logic through ATPG (Automatic Test Pattern Generation Vectors).
- Dedicated test logic for the on-chip custom memory macros to provide complete coverage on these modules.

- A JTAG test mode to allow board level testing of neighboring devices.
- An EXOR tree test mode on all the digital I/O's to allow for proper soldering verification at the board level.
- A VOH/VOL test mode on all digital I/O’s to allow for proper verification of output high and output low values at the board level.
- Access to the analog modules to allow full evaluation and characterization.
- IDDQ mode support to allow chip evaluation through current leakage measurements.

These test modes can be accessed through the settings on the instruction register of the JTAG circuitry.

### 1.2.8 Packaging

- Single chip solution in 55nm, 1.1V low power CMOS technology.
- 528-FCBGA package, 21mmx21mm.

## 1.3 Software Features

- Supports Microsoft Windows XP, Windows Vista, and Windows 7.
- Supports corporate manageability requirements such as DMI.
- ACPI support.
- Full Write Combining support for maximum performance of the CPU.
- Comprehensive OS and API support.
- Hot-key support (Windows ACPI 2.0 or AMD Event Handler Utility where appropriate).
- Extensive power management support.
- Supports AMD OverDrive™ utility.

*****Warning***** AMD and ATI processors are intendedto be operated only within their associated specifications and factory settings. Operating the AMD or ATI processor outside of specification or in excess of factory settings, including but not limited to overclocking, may damage the processor and/or lead to other problems, including but not limited to, damage to the system components (including the motherboard and components thereon (e.g. memory)), system instabilities (e.g. data loss and corrupted images), shortened processor, system component and/or system life and in extreme cases, total system failure. AMD does not provide support or service for issues or damages related to use of an AMD or ATI processor outside of processor specifications or in excess of factory settings.

## 1.4 Branding Diagram

**Note:** The branding can be in laser, ink, or mixed laser-and-ink marking.

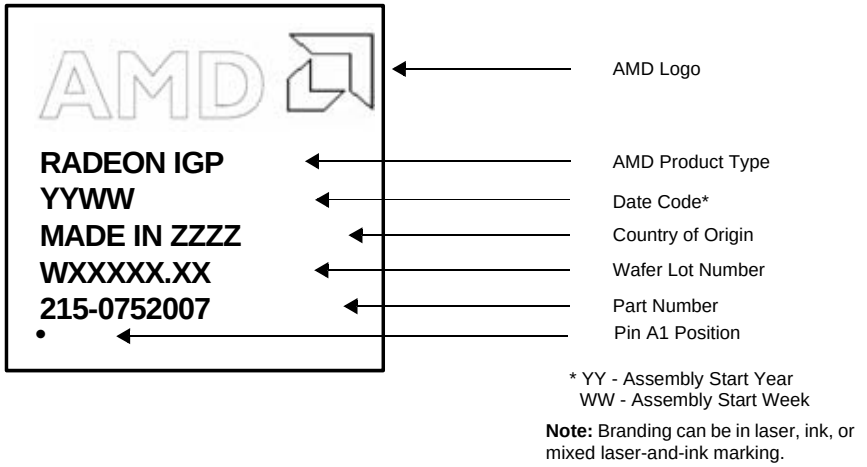


**Figure 1-1 RX881 ASIC A11 Production Branding**

## 1.5 Conventions and Notations

The following conventions are used throughout this manual.

### 1.5.1 Pin Names

Pins are identified by their pin names or ball references. Multiplexed pins sometimes assume alternate “functional names” when they perform their alternate functions, and these “functional names” are given in *Chapter 3, “Pin Descriptions and Strap Options.”*

All active-low signals are identified by the suffix ‘#’ in their names (e.g., MEM_RAS#).

### 1.5.2 Pin Types

The pins are assigned different codes according to their operational characteristics. These codes are listed in *Table 1-2*.

**Table 1-2 Pin Type Codes**

| Code | Pin Type |
|---|---|
| I | Digital Input |
| O | Digital Output |
| OD | Open Drain |
| I/O | Bi-Directional Digital Input or Output |
| I/OD | Digital Input or Open Drain |
| M | Multifunctional |
| Pwr | Power |
| Gnd | Ground |
| A-O | Analog Output |
| A-I | Analog Input |
| A-I/O | Analog Bi-Directional Input/Output |
| A-Pwr | Analog Power |
| A-Gnd | Analog Ground |
| Other | Pin types not included in any of the categories above |

### 1.5.3 Numeric Representation

Hexadecimal numbers are appended with “h” (Intel assembly-style notation) whenever there is a risk of ambiguity. Other numbers are in decimal.

Pins of identical functions but different running integers (e.g., “GFX_TX7P, GFX_TX6P,... GFX_TX0P”) are referred to collectively by specifying their integers in square brackets and with colons (i.e., “GFX_TX[7:0]P”). A similar short-hand notation is used to indicate bit occupation in a register. For example, NB_COMMAND[15:10] refers to the bit positions 10 through 15 of the NB_COMMAND register.

### 1.5.4 Register Field

A field of a register is referred to by the format of [Register Name].[Register.Field]. For example, “NB_MC_CNTL.DISABLE_BYPASS” is the “DISABLE_BYPASS” field of the register “NB_MC_CNTL.”

### 1.5.5 Hyperlinks

Phrases or sentences in *blue italic font* are hyperlinks to other parts of the manual. Users of the PDF version of this manual can click on the links to go directly to the referenced sections, tables, or figures.

### 1.5.6 Acronyms and Abbreviations

The following is a list of the acronyms and abbreviations used in this manual.

**Table 1-3 Acronyms and Abbreviations**

| Acronym | Full Expression |
|---|---|
| ACPI | Advanced Configuration and Power Interface |
| A-Link-E | A-Link Express interface between the IGP and the Southbridge. |
| BGA | Ball Grid Array |
| BIOS | Basic Input Output System. Initialization code stored in a ROM or Flash RAM used to start up a system or expansion card. |
| BIST | Built In Self Test. |
| CSP | Chip Scale Package |
| DBI | Dynamic Bus Inversion |
| DFP | Digital Flat Panel. Monitor connection standard from VESA. |
| DPM | Defects per Million |
| EPROM | Erasable Programmable Read Only Memory |
| FIFO | First In, First Out |
| GND | Ground |
| GPIO | General Purpose Input/Output |
| IDDQ | Direct Drain Quiescent Current |
| JTAG | Joint Test Access Group. An IEEE standard. |
| MB | Mega Byte |
| PCI | Peripheral Component Interface |
| PCIe | PCI Express |
| PLL | Phase Locked Loop |
| POST | Power On Self Test |
| PD | Pull-down Resistor |
| PU | Pull-up Resistor |
| SDRAM | Synchronous Dynamic RAM |
| VRM | Voltage Regulation Module |

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# Chapter 2
# Functional Descriptions

This chapter describes the functional operation of the major interfaces of the RX881 system logic. *Figure 2-1, "RX881 Internal Block Diagram,"* illustrates the RX881 internal blocks and interfaces.

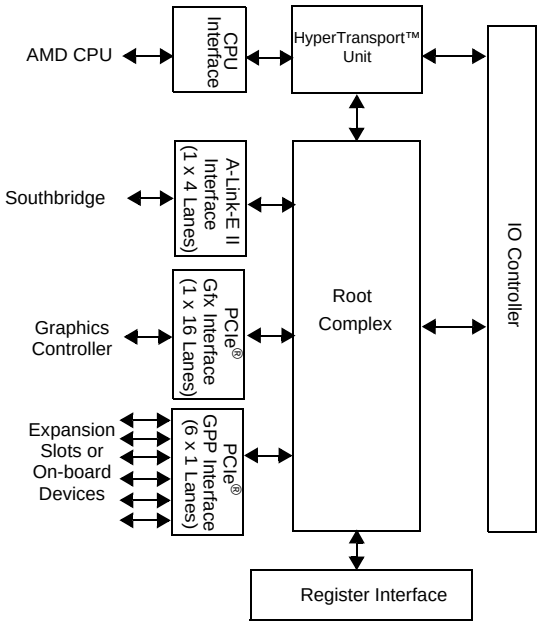


**Figure 2-1 RX881 Internal Block Diagram**

## 2.1 Host Interface

The RX881 is optimized to interface with AMD processors through the HyperTransport™ interface. This section presents an overview of the HyperTransport interface. For a detailed description of the interface, please refer to the *HyperTransport I/O Link Specification* from the HyperTransport Consortium. *Figure 2-2, "Host Interface Block Diagram,"* illustrates the basic blocks of the host bus interface of the RX881.

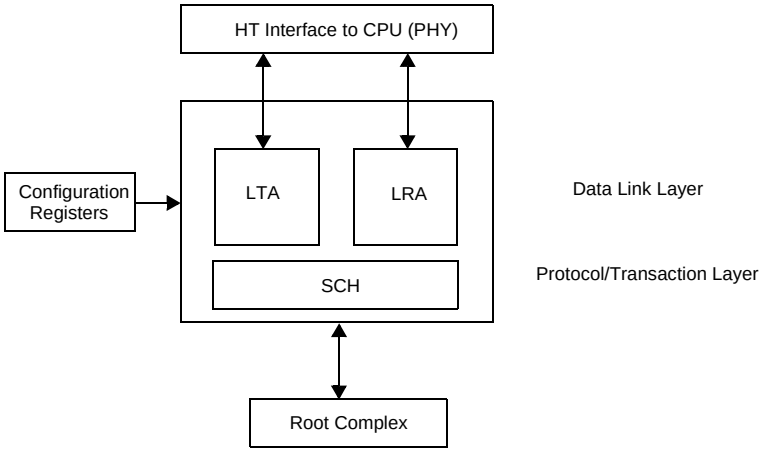


**Figure 2-2 Host Interface Block Diagram**

The HyperTransport (HT) Interface, formerly known as the LDT (Lightning Data Transport) interface, is a high speed, packet-based link implemented on two unidirectional buses. It is a point-to-point interface where data can flow both upstream and downstream at the same time. The commands, addresses, and data travel in packets on the HyperTransport link. Lengths of packets are in multiples of four bytes. The HT link consists of three parts: the physical layer (PHY), the data link layer, and the protocol/transaction layer. The PHY is the physical interface between the RX881 and the CPU. The data link layer includes the initialization and configuration sequences, periodic redundancy checks, connect/disconnect sequences, and information packet flow controls. The protocol layer is responsible for maintaining strict ordering rules defined by the HT protocol.

The RX881 HyperTransport bus interface consists of eighteen unidirectional differential data/control pairs and two differential clock pairs in each of the upstream and downstream direction. On power up, the HT link is 8-bit wide and runs at a default speed of 400MT/s. After negotiation, carried out by the HW and SW together, the link width can be brought up to 16-bit and the interface can run up to 4.4GT/s. The interface is illustrated in *Figure 2-3, "RX881 Host Bus Interface Signals."* The signal name and direction for each signal is shown with respect to the processor. Note that the signal names may be different from those used in the pin listing of the RX881. Detailed descriptions of the signals are given in *section 3.3, "CPU HyperTransport™ Interface,' on page 3-5*.

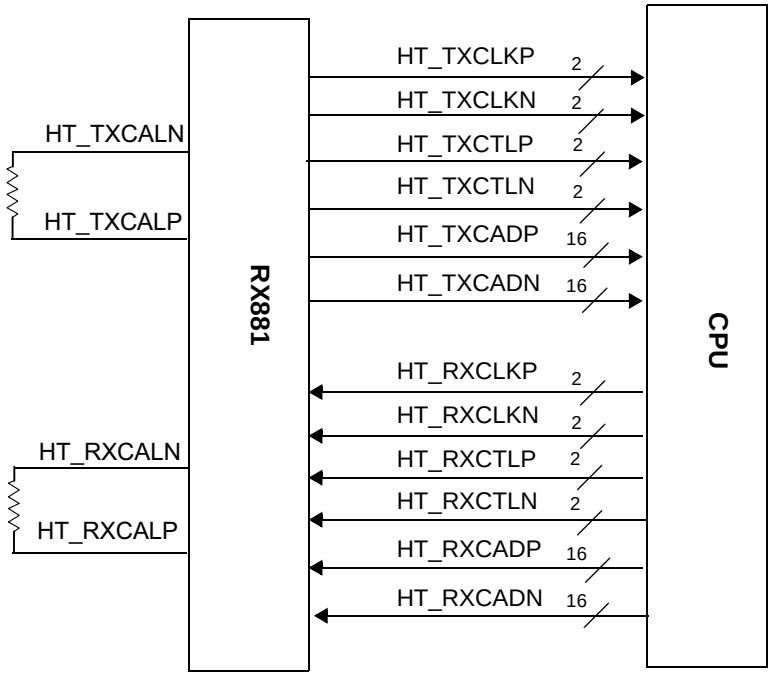


**Figure 2-3 RX881 Host Bus Interface Signals**

## 2.2 Clock Generation

The RX881 provides support for an external clock chip to generate PCIe and A-Link Express II clocks.

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# Chapter 3
# Pin Descriptions and Strap Options

This chapter gives the pin descriptions and the strap options for the RX881. To jump to a topic of interest, use the following list of hyperlinked cross references:

## 3.1 RX881 Pin Assignment Top View

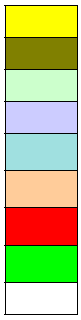
The figures below only represent the relative ball positions. For the actual physical layout of the balls, please refer to *Figure 5-2, "RX881 Ball Arrangement (Bottom View)," on page 5- 6*.

| | 1 | 2 | 3 | 4 | 5 | 6 | 7 | 8 | 9 | 10 | 11 | 12 | 13 |
|---|---|---|---|---|---|---|---|---|---|---|---|---|---|
| A | | VSSAPCIE | GFX_RX1P | GFX_TX1P | GFX_TX0P | VDDPCIE | NC | NC | NC | POWERGOOD | DAC_HSYNC | PLLVDD | VDDLTP18 |
| B | VSSAPCIE | GFX_TX2N | GFX_RX1N | GFX_TX1N | GFX_TX0N | VDDPCIE | NC | NC | NC | STRP_DATA | DAC_VSYNC | PLLVSS | VSSLTP18 |
| C | GFX_RX2N | GFX_RX2P | GFX_TX2P | GFX_RX0N | | VDDPCIE | | NC | | LDTSTOP# | | ALLOW_LDTSTOP | |
| D | GFX_TX3P | GFX_TX3N | VSSAPCIE | GFX_RX0P | VSSAPCIE | VDDPCIE | VDDA18PCIEPLL | SYSRESET# | NC | NC | VSS | SUS_STAT# | TESTMODE |
| E | GFX_TX4N | GFX_TX4P | | VSSAPCIE | GFX_RX3P | VDDPCIE | VDDA18PCIEPLL | NC | GPIO3 | | REFCLK_P | AVDD | |
| F | GFX_TX6P | GFX_TX6N | GFX_TX5N | GFX_TX5P | GFX_RX3N | VDDPCIE | GPIO2 | NC | VDD18 | | REFCLK_N | AVDD | |
| G | VSSAPCIE | VSSAPCIE | | VSSAPCIE | GFX_RX4P | GFX_RX4N | VDDPCIE | VSS | VDD18 | | RESERVED | GPIO4 | |
| H | GFX_TX8P | GFX_TX8N | GFX_TX7N | GFX_TX7P | GFX_RX5P | GFX_RX5N | VSSAPCIE | VDDPCIE | VDDA18PCIE | | VDD33 | VDD33 | |
| J | GFX_TX9N | GFX_TX9P | | VSSAPCIE | GFX_RX6N | GFX_RX6P | GFX_RX7P | GFX_RX7N | VDDPCIE | VDDA18PCIE | VDDC | VSS | |
| K | GFX_TX11P | GFX_TX11N | GFX_TX10N | GFX_TX10P | | | | | VDDPCIE | VDDA18PCIE | VSS | VDDC | |
| L | VSSAPCIE | VSSAPCIE | | VSSAPCIE | GFX_RX8P | GFX_RX8N | VSSAPCIE | GFX_RX9N | VDDPCIE | VDDA18PCIE | VDDC | VSS | |
| M | GFX_TX13P | GFX_TX13N | GFX_TX12N | GFX_TX12P | GFX_RX11N | VSSAPCIE | GFX_RX10N | GFX_RX9P | VDDPCIE | VDDA18PCIE | VSS | VDDC | VDDC |
| N | GFX_TX14N | GFX_TX14P | | VSSAPCIE | | | | | | | | VDDC | VSS |
| P | GFX_TX15P | GFX_TX15N | GFX_RX14N | GFX_RX14P | GFX_RX11P | VSSAPCIE | GFX_RX10P | GFX_RX12N | VDDPCIE | VDDA18PCIE | VDDC | VSS | VDDC |
| R | VSSAPCIE | VSSAPCIE | | VSSAPCIE | GFX_RX13N | GFX_RX13P | VSSAPCIE | GFX_RX12P | VDDPCIE | VDDA18PCIE | VSS | VDDC | |
| T | GFX_REFCLKN | GFX_REFCLKP | GFX_RX15N | GFX_RX15P | | | | | VDDPCIE | VDDA18PCIE | VDDC | VSS | |
| U | GPP_REFCLKP | GPP_REFCLKN | | VSSAPCIE | GPP_RX4P | GPP_RX4N | GPP_RX5N | GPP_RX5P | VDDPCIE | VDDA18PCIE | VSS | VDDC | |
| V | GPP_TX5P | GPP_TX5N | GPPSB_REFCLKN | GPPSB_REFCLKP | GPP_RX3P | VSSAPCIE | VSSAPCIE | VSSAPCIE | VDDPCIE | | NC | VSS | |
| W | VSSAPCIE | VSSAPCIE | | VSSAPCIE | SB_RX3P | GPP_RX3N | VSSAPCIE | VSSAPCIE | VDDA18PCIE | | VSS | NC | |
| Y | GPP_TX3P | GPP_TX3N | GPP_TX4N | GPP_TX4P | SB_RX3N | VSSAPCIE | SB_RX1N | SB_RX0N | VDDA18PCIE | | VDD_MEM | NC | |
| AA | GPP_TX2N | GPP_TX2P | | VSSAPCIE | SB_RX2P | SB_RX2N | SB_RX1P | SB_RX0P | VDDA18PCIE | | VDD_MEM | NC | |
| AB | VSSAPCIE | VSSAPCIE | GPP_TX1N | GPP_TX1P | VSSAPCIE | SB_TX2P | VSSAPCIE | PCE_CALRN | VDDA18PCIE | VDD_MEM | VSS | NC | NC |
| AC | GPP_TX0P | GPP_TX0N | VSSAPCIE | VSSAPCIE | | SB_TX2N | | PCE_CALRP | | VDD_MEM | | VSS | |
| AD | GPP_RX2P | GPP_RX2N | GPP_RX1N | GPP_RX0N | SB_TX3P | SB_TX1N | SB_TX0P | THERMALDIODE_N | VDDA18PCIE | VDD_MEM | VDD18_MEM | NC | NC |
| AE | VSSAPCIE | GPP_RX1P | GPP_RX0P | VSSAPCIE | SB_TX3N | SB_TX1P | SB_TX0N | THERMALDIODE_P | VDDA18PCIE | VDD_MEM | VDD18_MEM | NC | NC |
| | 1 | 2 | 3 | 4 | 5 | 6 | 7 | 8 | 9 | 10 | 11 | 12 | 13 |

CPU Interface
A-Link Express II Interface
Clock Interface
External graphics Interface
General Purpose External Device Interface
Power Management Interface
Powers
Grounds
Others

**Figure 3-1 RX881 Pin Assignment Top View (Left)**

| 14 | 15 | 16 | 17 | 18 | 19 | 20 | 21 | 22 | 23 | 24 | 25 | |
|---|---|---|---|---|---|---|---|---|---|---|---|---|
| VDDLT33 | VDDLT18 | NC | NC | NC | NC | NC | NC | NC | VDDHTRX | HT_RXCALN | VSSAHT | A |
| VDDLT33 | VDDLT18 | NC | NC | NC | NC | NC | NC | NC | VDDHTRX | HT_TXCALP | HT_TXCALN | B |
| VSSLT | | VSSLT | | VSSLT | | VSSLT | | VSSLT | HT_RXCALP | HT_REFCLKN | HT_REFCLKP | C |
| PLLVDD18 | VSSLT | NC | NC | NC | NC | NC | NC | VDDHTRX | VSSAHT | HT_TXCAD0P | HT_TXCAD0N | D |
| VSS | VSS | | NC | NC | NC | VSSLT | VDDHTRX | VSSAHT | | HT_TXCAD1P | HT_TXCAD1N | E |
| AVDDDI | NC | | NC | VSS | VSS | VDDHTRX | HT_TXCAD8P | HT_TXCAD3N | HT_TXCAD3P | HT_TXCAD2P | HT_TXCAD2N | F |
| NC | AVSSDI | | VSS | NC | VDDHTRX | HT_TXCAD9P | HT_TXCAD8N | VSSAHT | | VSSAHT | VSSAHT | G |
| AVSSQ | AVDDQ | | VDDA18HTPLL | VDDHTRX | VSSAHT | VSSAHT | HT_TXCAD9N | HT_TXCAD4N | HT_TXCAD4P | HT_TXCLK0P | HT_TXCLK0N | H |
| VDDC | VSS | VDDC | VDDHT | HT_TXCAD11P | HT_TXCAD12N | HT_TXCAD10P | HT_TXCAD10N | VSSAHT | | HT_TXCAD5N | HT_TXCAD5P | J |
| VSS | VDDC | VDDHT | HT_TXCAD11N | | | | | HT_TXCAD7N | HT_TXCAD7P | HT_TXCAD6P | HT_TXCAD6N | K |
| VDDC | VSS | VDDHT | VSSAHT | HT_TXCAD13N | HT_TXCAD12P | HT_TXCLK1N | HT_TXCLK1P | VSSAHT | | VSSAHT | VSSAHT | L |
| VSS | VDDC | VDDHT | VDDHTTX | HT_TXCAD15N | HT_TXCAD13P | VSSAHT | HT_TXCAD14P | HT_RXCTL0P | HT_RXCTL0N | HT_TXCTL0P | HT_TXCTL0N | M |
| VDDC | | | | | | | | VSSAHT | | HT_RXCAD7P | HT_RXCAD7N | N |
| VDDC | VSS | VDDHT | VDDHTTX | HT_TXCAD15P | HT_TXCTL1P | VSSAHT | HT_TXCAD14N | HT_RXCAD5P | HT_RXCAD5N | HT_RXCAD6N | HT_RXCAD6P | P |
| VSS | VDDC | VDDHT | VDDHTTX | HT_TXCTL1N | VSSAHT | HT_RXCTL1N | HT_RXCTL1P | VSSAHT | | VSSAHT | VSSAHT | R |
| VDDC | VDDC | VDDHT | VDDHTTX | | | | | HT_RXCLK0P | HT_RXCLK0N | HT_RXCAD4N | HT_RXCAD4P | T |
| VSS | VSS | VDDC | VDDHTTX | HT_RXCAD15 | HT_RXCAD15 | HT_RXCAD14 | HT_RXCAD14 | VSSAHT | | HT_RXCAD3P | HT_RXCAD3N | U |
| NC | NC | | NC | VDDHTTX | VSSAHT | HT_RXCAD13 | HT_RXCAD13 | HT_RXCAD1P | HT_RXCAD1N | HT_RXCAD2N | HT_RXCAD2P | V |
| NC | VSS | | NC | NC | VDDHTTX | HT_RXCAD12 | HT_RXCAD12 | VSSAHT | | VSSAHT | VSSAHT | W |
| NC | NC | | NC | VSS | NC | VDDHTTX | VSSAHT | HT_RXCAD11P | HT_RXCAD11 | HT_RXCAD0N | HT_RXCAD0P | Y |
| VSS | NC | | NC | NC | NC | NC | VDDHTTX | HT_RXCLK1N | | HT_RXCAD10 | HT_RXCAD10 | AA |
| NC | VSS | NC | VSS | NC | VSS | NC | VSS | VDDHTTX | HT_RXCLK1P | HT_RXCAD9N | HT_RXCAD9P | AB |
| NC | | NC | | NC | | NC | | NC | VDDHTTX | HT_RXCAD8P | HT_RXCAD8N | AC |
| NC | NC | NC | NC | NC | NC | NC | NC | NC | IOPLLVSS | VDDHTTX | VSSAHT | AD |
| VSS | NC | NC | NC | MEM_VREF | NC | VSS | NC | NC | IOPLLVDD18 | IOPLLVDD | VDDHTTX | AE |
| 14 | 15 | 16 | 17 | 18 | 19 | 20 | 21 | 22 | 23 | 24 | 25 | |



CPU Interface
A-Link Express II Interface
Clock Interface
External graphics Interface
General Purpose External Device Interface
Power Management Interface
Powers
Grounds
Others

**Figure 3-2 RX881 Pin Assignment Top View (Right)**

## 3.2 Interface Block Diagram

Figure 3-3 shows the different interfaces on the RX881. Interface names in blue are hyperlinks to the corresponding sections in this chapter.

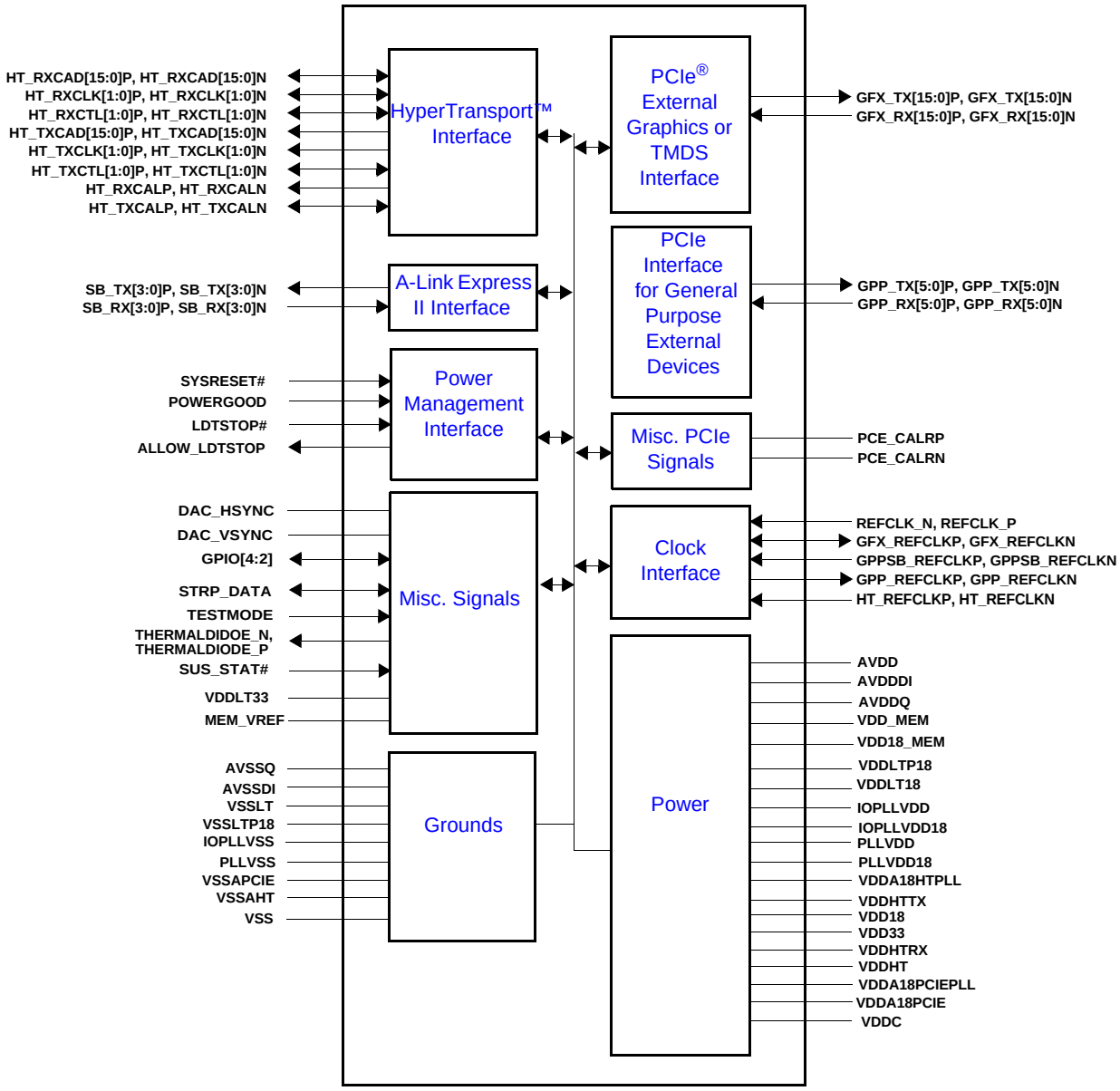



**Figure 3-3 RX881 Interface Block Diagram**

## 3.3 CPU HyperTransport™ Interface

**Table 3-1 CPU HyperTransport™ Interface**

| Pin Name | Type | Power Domain | Ground Domain | Functional Description |
|---|---|---|---|---|
| HT_RXCAD[15:0]P, HT_RXCAD[15:0]N | I | VDDHTRX | VSS | Receiver Command, Address, and Data Differential Pairs |
| HT_RXCLK[1:0]P, HT_RXCLK[1:0]N | I | VDDHTRX | VSS | Receiver Clock Signal Differential Pairs. Forwarded clock signal. Each byte of RXCAD uses a different clock signal. Data is transferred on each clock edge. |
| HT_RXCTL[1:0]P, HT_RXCTL[1:0]N | I | VDDHTRX | VSS | Receiver Control Differential Pairs. For distinguishing control packets from data packets. |
| HT_TXCAD[15:0]P, HT_TXCAD[15:0]N | O | VDDHTTX | VSS | Transmitter Command, Address, and Data Differential Pairs |
| HT_TXCLK[1:0]P, HT_TXCLK[1:0]N | O | VDDHTTX | VSS | Transmitter Clock Signal Differential Pairs. Each byte of TXCAD uses a different clock signal. Data is transferred on each clock edge. |
| HT_TXCTL[1:0]P, HT_TXCTL[1:0]N | O | VDDHTTX | VSS | Transmitter Control Differential Pairs. Forwarded clock signal. For distinguishing control packets from data packets. |
| HT_RXCALN | Other | VDDHTRX | VSS | Receiver Calibration Resistor to VDD_HT power rail. |
| HT_RXCALP | Other | VDDHTRX | VSS | Receiver Calibration Resistor to Ground |
| HT_TXCALP | Other | VDDHTTX | VSS | Transmitter Calibration Resistor to HTTX_CALN |
| HT_TXCALN | Other | VDDHTTX | VSS | Transmitter Calibration Resistor to HTTX_CALP |

## 3.4 PCI Express® Interfaces

### 3.4.1 1 x 16 Lane Interface for External Graphics

**Table 3-2 1 x 16 Lane PCI Express® Interface for External Graphics**

| Pin Name | Type | Power Domain | Ground Domain | Integrated Termination | Functional Description |
|---|---|---|---|---|---|
| GFX_TX[15:0]P, GFX_TX[15:0]N | O | VDDPCIE | VSSAPCIE | 50Ω between complements | Transmit Data Differential Pairs. Connect to external connector for an external graphics card on the motherboard (if implemented). |
| GFX_RX[15:0]P, GFX_RX[15:0]N | I | VDDPCIE | VSSAPCIE | 50Ω between complements | Receive Data Differential Pairs. Connect to external connector for an external graphics card on the motherboard (if implemented). |

### 3.4.2 A-Link Express II Interface for Southbridge

**Note:** The widths of the A-Link Express II interface and the general purpose links for external devices are configured through the programmable strap GPPSB_LINK_CONFIG, which is programmed through RX881's registers. See the *RS880 ASIC Family Register Reference Guide*, order# 46142, and the *RS880 ASIC Family Register Programming Requirements*, order# 46141, for details.

**Table 3-3 1 x 4 Lane A-Link Express II Interface for Southbridge**

| Pin Name | Type | Power Domain | Ground Domain | Integrated Termination | Functional Description |
|---|---|---|---|---|---|
| SB_TX[3:0]P, SB_TX[3:0]N | O | VDDPCIE | VSSAPCIE | 50Ω between complements | Transmit Data Differential Pairs. Connect to the corresponding Receive Data Differential pairs on the Southbridge. |
| SB_RX[3:0]P, SB_RX[3:0]N | I | VDDPCIE | VSSAPCIE | 50Ω between complements | Receive Data Differential Pairs. Connect to the corresponding Transmit Data Differential pairs on the Southbridge. |

### 3.4.3 6 x 1 Lane Interface for General Purpose External Devices

**Note:** The widths of the A-Link Express II interface and the general purpose links for external devices are configured through the programmable strap GPPSB_LINK_CONFIG, which is programmed through RX881's registers. See the *RS880 ASIC Family Register Reference Guide*, order# 46412, and the *RS880 ASIC Family Register Programming Requirements*, order# 46141, for details.

**Table 3-4 6 x 1 Lane PCI Express® Interface for General Purpose External Devices**

| Pin Name | Type | Power Domain | Ground Domain | Integrated Termination | Functional Description |
|---|---|---|---|---|---|
| GPP_TX[5:0]P, GPP_TX[5:0]N | O | VDDPCIE | VSSAPCIE | 50Ω between complements | Transmit Data Differential Pairs. Connect to external connectors on the motherboard for add-in card or ExpressCard support. |
| GPP_RX[5:0]P, GPP_RX[5:0]N | I | VDDPCIE | VSSAPCIE | 50Ω between complements | Receive Data Differential Pairs. Connect to external connectors on the motherboard for add-in card or ExpressCard support. |

### 3.4.4 Miscellaneous PCI Express® Signals

**Table 3-5 PCI Express® Interface for Miscellaneous PCI Express® Signals**

| Pin Name | Type | Power Domain | Ground Domain | Functional Description |
|---|---|---|---|---|
| PCE_CALRN | Other | VDDPCIE | VSSAPCIE | RX Impedance Calibration. Connect to VDDPCIE on the motherboard with an external resistor of an appropriate value. |
| PCE_CALRP | Other | VDDPCIE | VSSAPCIE | TX Impedance Calibration. Connect to GND on the motherboard with an external resistor of an appropriate value. |

## 3.5 Clock Interface

**Table 3-6 Clock Interface**

| Pin Name | Type | Power Domain | Ground Domain | Integrated Termination | Functional Description |
|---|---|---|---|---|---|
| HT_REFCLKP, HT_REFCLKN | I | VDDA18HTPLL | VSSAHT | – | HyperTransport™ 100MHz reference clock differential pair<br>**External clock mode:** Input from external clock source, as a reference clock for the HyperTransport interface.<br>**Internal clock mode*:** Input from the SB8xx Southbridge, as a reference clock for the HyperTransport interface. |
| GFX_REFCLKP, GFX_REFCLKN | I/O | VDDPCIE | VSSAPCIE | 50Ω between complements | Clock Differential Pair for external graphics.<br>**External clock mode:** Input from the external clock generator, as a reference clock for external graphics.<br>**Internal clock mode*:** Not used. Pull down following instructions in the *RS880-Series IGP Motherboard Schematic Review Checklist.* |
| GPPSB_REFCLKP, GPPSB_REFCLKN | I | VDDPCIE | VSSAPCIE | 50Ω between complements | Clock Differential Pair for Southbridge and general purpose PCIe® devices.<br>**External clock mode:** Input from the external clock generator, as a reference clock for A-Link Express II and general purpose PCIe.<br>**Internal clock mode*:** Input from the SB8xx Southbridge, as a reference clock for A-Link II and general purpose PCIe. |
| GPP_REFCLKP, GPP_REFCLKN | O | VDDPCIE | VSSAPCIE | 50Ω between complements | Clock Differential Pair for general purpose PCIe devices.<br>**External clock mode:** Not used. Can be left unconnected, or connected to the external clock generator for maintaining system compatibility with the RX881.<br>**Internal clock mode*:** Output to a GPP device slot as a GPP clock. |
| REFCLK_P, REFCLK_N | I | VDD33 | VSS | – | Do not connect. |

***Note:** Internal clock mode is only available when using an SB8xx Southbridge. Use of the internal clock generator function is subject to characterization with actual RX881 and SB8xx devices

## 3.6 Power Management Pins

**Table 3-7 Power Management Pins**

| Pin Name | Type | Power Domain | Ground Domain | Functional Description |
|---|---|---|---|---|
| LDTSTOP# | I | VDD33 | VSS | HyperTransport™ Stop. Used for systems requiring power management. It is a single-ended signal for input from the Southbridge to enable and disable the HyperTransport link during system state transitions.<br>**Note:** For platforms supporting DDR2 system memory, 1.8V signalling can be used on the signal. For platforms supporting DDR3 system memory, follow recommendations in the *RS880-Series IGP Motherboard Schematic Review Checklist.* |
| ALLOW_LDTSTOP | OD | VDD33 | VSS | Allow LDTSTOP. The signal is used for controlling LDTSTOP assertions. It is an output to the SB.<br>1 = LDTSTOP# can be asserted<br>0 = LDTSTOP# has to be de-asserted<br>**Note:** For platforms supporting DDR2 system memory, 1.8V signalling can be used on the signal. For platforms supporting DDR3 system memory, follow recommendations in the *RS880-Series IGP Motherboard Schematic Review Checklist.* |
| SYSRESET# | I | VDD33 | VSS | Global Hardware Reset. This signal comes from the Southbridge. |
| POWERGOOD | I | VDD18 | VSS | Input from the motherboard signifying that the power to the RX881 is up and ready. Signal High means all power planes are valid. It is not observed internally until it has been high for more than six consecutive REFCLK cycles. The rising edge of this signal is deglitched. |

## 3.7 Miscellaneous Pins

**Table 3-8 Miscellaneous Pins**

| Pin Name | Type | Power Domain | Ground Domain | Integrated Termination | Functional Description |
|---|---|---|---|---|---|
| DAC_HSYNC | Other | VDD33 | VSS | 50kΩ programmable: PU/PD/none | This is a strap pin for a reserved strap function. See *Table 3-11, "Strap Definitions for the RX881,"* for details. |
| DAC_VSYNC | Other | VDD33 | VSS | 50kΩ programmable: PU/PD/none | This is a strap pin for the STRAP_DEBUG_BUS_GPIO _ENABLE# strap function. See *Table 3-11, "Strap Definitions for the RX881,"* for details. |
| GPIO[4:2] | I/O | VDDR3 | VSS | 50kΩ programmable: PU/PD/none | General Purpose I/O. These pins can also be used as outputs to the voltage regulator for pulse-width modulation of various voltages on the motherboard. |
| MEM_VREF | Other | – | VSS | None | Connect the pin to ground |
| NC | – | – | – | – | No connect. These pins should be left unconnected to anything. |
| STRP_DATA | I/O | VDD33 | VSS | 50kΩ programmable: PU/PD/none | $I^2C$ interface data signal for external EEPROM based strap loading. Can also be used as GPIO, or as output to the voltage regulator for pulse-width modulation of RX881's core voltage. |
| SUS_STAT# | Other | VDD33 | VSS | 50kΩ programmable: PU/PD/none | This is a strap pin for the LOAD_EEPROM_STRAPS# strap function. See *Table 3-11, "Strap Definitions for the RX881,"* for details. |
| TESTMODE | I | VDD33 | VSS | – | When High, puts the RX881 in test mode and disables the RX881 from operating normally. |

**Table 3-8 Miscellaneous Pins (Continued)**

| Pin Name | Type | Power Domain | Ground Domain | Integrated Termination | Functional Description |
|---|---|---|---|---|---|
| THERMALDIODE_P, THERMALDIODE_N | A-O | – | – | – | Diode connections to external SMBus microcontroller for monitoring IC thermal characteristics. |
| VDDLT33 | Other | – | – | – | These balls are only for maintaining pin-compatibility with earlier generations of AMD IGPs or chipsets. They can either be connected to a 3.3V rail or left unconnected on RX881 systems. |

## 3.8 Power Pins

**Table 3-9 Power Pins**

| Pin Name | Voltage | Pin Count | Ball Reference | Pin Description |
|---|---|---|---|---|
| AVDD | 3.3V | 2 | E12, F12 | Connect these pins to ground. |
| AVDDDI | 1.8V | 1 | F14 | Connect the pin to ground. |
| AVDDQ | 1.8V | 1 | H15 | Connect the pin to ground. |
| IOPLLVDD | 1.1V | 1 | AE24 | Connect the pin to a 1.1V power rail. |
| IOPLLVDD18 | 1.8V | 1 | AE23 | Connect the pin to the VDD18 power rail. |
| PLLVDD | 1.V | 1 | A12 | Connect the pin to ground. |
| PLLVDD18 | 1.8V | 1 | D14 | Connect the pin to ground. |
| VDD_MEM | 1.5/1.8V | 6 | AA11, AB10, AC10, AD10, AE10, Y11 | Connect these pins to ground. |
| VDD18_MEM | 1.8V | 2 | AD11, AE11 | Connect these pins ground. |
| VDDA18HTPLL | 1.8V | 1 | H17 | I/O power for HyperTransport PLL |
| VDDA18PCIE | 1.8V | 15 | AA9, AB9, AD9, AE9, H9, J10, K10, L10, M10, P10, R10, T10, U10, W9, Y9 | 1.8V I/O power for PCIe graphics, SB, and GPP interfaces |
| VDDA18PCIEPLL | 1.8V | 2 | D7, E7 | 1.8V I/O power for PCIe PLLs |
| VDDC | 1.1V | 22 | J11, J14, J16, K12, K15, L11, L14, M12, M13, M15, N12, N14, P11, P13, P14, R12, R15, T11, T14, T15, U12, U16 | Core power |
| VDD18 | 1.8V | 2 | F9, G9 | 1.8V I/O transform power |
| VDD33 | 3.3V | 2 | H11, H12 | 3.3V I/O power |
| VDDHT | 1.1V | 7 | J17, K16, L16, M16, P16, R16, T16 | Digital I/O power for HyperTransport interface |
| VDDHTRX | 1.1V | 7 | A23 ,B23, D22, E21, F20, G19, H18 | I/O power for HyperTransport receive interface |
| VDDHTTX | 1.2V | 13 | AA21, AB22, AC23, AD24, AE25, M17, P17, R17, T17, U17, V18, W19, Y20 | I/O power for HyperTransport transmit interface |
| VDDLT18 | 1.8V | 2 | A15, B15 | Connect these pins to ground |
| VDDLTP18 | 1.8V | 1 | A13 | Connect the pin to ground |
| VDDPCIE | 1.1V | 17 | A6, B6, C6, D6, E6, F6, G7, H8, J9, K9, L9, M9, P9, R9, T9, U9, V9 | Main I/O power for PCIe graphics, SB, and GPP interfaces |
| Total Power Pin Count | | 107 | | |

## 3.9 Ground Pins

**Table 3-10 Ground Pins**

| Pin Name | Pin Count | Ball Reference | Comments |
|---|---|---|---|
| AVSSDI | 1 | G15 | Connect the pin to common ground. |
| AVSSQ | 1 | H14 | Connect the pin to common ground. |
| IOPLLVSS | 1 | AD23 | Connect the pin to common ground. |
| PLLVSS | 1 | B12 | Connect the pin to common ground. |
| VSS | 37 | AA14, AB11, AB15, AB17, AB19, AB21, AC12, AE14, AE20, D11, E14, E15, F18, F19, G17, G8, J12, J15, K11, K14, L12, L15, M11, M14, N13, P12, P15, R11, R14, T12, U11, U14, U15, V12, W11, W15, Y18 | Common Ground |
| VSSAHT | 27 | A25, AD25, D23, E22, G22, G24, G25, H19, H20, J22, L17, L22, L24, L25, M20, N22, P20, R19, R22, R24, R25, U22, V19, W22, W24, W25, Y21 | Ground pin for HyperTransport interface PLL |
| VSSAPCIE | 40 | A2, AA4, AB1, AB2, AB5, AB7, AC3, AC4, AE1, AE4, B1, D3, D5, E4, G1, G2, G4, H7, J4, L1, L2, L4, L7, M6, N4, P6, R1, R2, R4, R7, U4, V6, V7, V8, W1, W2, W4, W7, W8, Y6 | Ground for PCI Express Interface |
| VSSLT | 7 | C14, C16, C18, C20, C22, D15, E20 | Connect these pins to common ground |
| VSSLTP18 | 1 | B13 | Connect the pin to common ground |
| Total Ground Pin Count | 116 | | |

## 3.10 Strapping Options

The RX881 provides strapping options to define specific operating parameters. The strap values are latched into internal registers after the assertion of the POWERGOOD signal to the RX881. *Table 3-11, "Strap Definitions for the RX881,"* shows the definitions of all the strap functions. These straps are set by one of the following four methods:

- Attaching pull-up resistors to specific strap pins listed in *Table 3-11* to set their values to "1".
- Attaching pull-down resistors to specific strap pins listed in *Table 3-11* to set their values to "0".
- Downloading the strap values from an $I^2C$ serial EEPROM (for debug purpose only; contact your AMD CSS representative for details).
- Setting through an external debug port, if implemented (contact your AMD CSS representative for details).

All of the straps listed in *Table 3-11* are defined active low. To select "1", the strap pins must be pulled up to VDD33 through resistors. To select "0", the strap pins must be pulled down to VSS through resistors. During reset, the strap pins are undriven, allowing the external pull-up or pull-down to pull a pin to "0" or "1." The values on the strap pins are then latched into the device and used as operational parameters. However, for debug purposes, those latched values may be overridden through an external debug strap port or by a bit-stream downloaded from a serial EEPROM.

**Table 3-11 Strap Definitions for the RX881**

| Strap Function | Strap Pin | Description |
|---|---|---|
| STRAP_DEBUG_BUS_GPIO_ENABLE# | DAC_VSYNC | Enables debug bus access through memory I/O pads and GPIOs.<br>0: Enable<br>1: Disable<br>(See debug bus specification documents for more details.) |
| RESERVED | DAC_HSYNC | 0: Reserved<br>1: Required setting. Select with a pull-up resistor on the strap**.** |
| LOAD_EEPROM_STRAPS# | SUS_STAT# | Selects loading of strap values from EEPROM.<br>0: $I^2C$ master can load strap values from EEPROM if connected, or use default values if EEPROM is not connected. Please refer to RX881's reference schematics for system level implementation details.<br>1: Use default values |

**Note**: On the RX881, the widths of the A-Link Express II interface and the general purpose PCIe links are configured through the programmable strap GPPSB_LINK_CONFIG, which is programmed through RX881's registers. See the *RS880 ASIC Family Register Reference Guide,* order# 46142, and the *RS880 ASIC Family Register Programming Requirements,* order# 46141, for details.

# Chapter 4
# Timing Specifications

## 4.1 HyperTransport™ Bus Timing

For HyperTransport™ bus timing information, please refer to CPU specifications.

## 4.2 HyperTransport™ Reference Clock Timing Parameters

**Table 4-1 Timing Requirements for HyperTransport™ Reference Clock (100MHz) Output by the Clock Generator**

| Symbol | Parameter | Minimum | Maximum | Unit | Note |
|---|---|---|---|---|---|
| $\Delta V_{CROSS}$ | Change in Crossing point voltage over all edges | - | 140 | mV | 1 |
| F | Frequency | 99.9 | 100 | MHz | 2 |
| ppm | Long Term Accuracy | -300 | +300 | Ppm | 3 |
| $S_{FALL}$ | Output falling edge slew rate | -10 | -0.5 | V/ns | 4, 5 |
| $S_{RISE}$ | Output rising edge slew rate | 0.5 | 10 | V/ns | 4, 5 |
| $T_{jc\ max}$ | Jitter, cycle to cycle | - | 150 | ps | 6 |
| $T_{j\text{-}accumulated}$ | Accumulated jitter over a 10 μs period | -1 | 1 | ns | 7 |
| $V_{D(PK\text{-}PK)}$ | Peak to Peak Differential Voltage | 400 | 2400 | mV | 8 |
| $V_D$ | Differential Voltage | 200 | 1200 | mV | 9 |
| $\Delta V_D$ | Change in $V_{DDC}$ cycle to cycle | -75 | 75 | mV | 10 |
| DC | Duty Cycle | 45 | 55 | % | 11 |

**Notes:**

More details are available in *AMD HyperTransport 3.0 Reference Clock Specification* and *AMD Family 10h Processor Reference Clock Parameters*, order # 34864.

1 Single-ended measurement at crossing point. Value is maximum-minimum over all time. DC value of common mode is not important due to blocking cap.

2 Minimum frequency is a consequence of 0.5% down spread spectrum.

3 Measured with spread spectrum turned off.

4 Only simulated at the receive die pad. This parameter is intended to give guidance for simulation. It cannot be tested on a tester but is guaranteed by design.

5 Differential measurement through the range of ±100mV, differential signal must remain monotonic and within slew rate specification when crossing through this region.

6 $T_{jc\ max}$ is the maximum difference of $t_{CYCLE}$ between any two adjacent cycles.

7 Accumulated $T_{jc}$ over a 10μs time period, measured with JIT2 TIE at 50ps interval.

8 $V_{D(PK\text{-}PK)}$ is the overall magnitude of the differential signal.

9 $V_{D(min)}$ is the amplitude of the ring-back differential measurement, guaranteed by design that the ring-back will not cross 0V $V_D$. $V_{D(max)}$ is the largest amplitude allowed.

10 The difference in magnitude of two adjacent $V_{DDC}$ measurements. $V_{DDC}$ is the stable post overshoot and ring-back part of the signal.

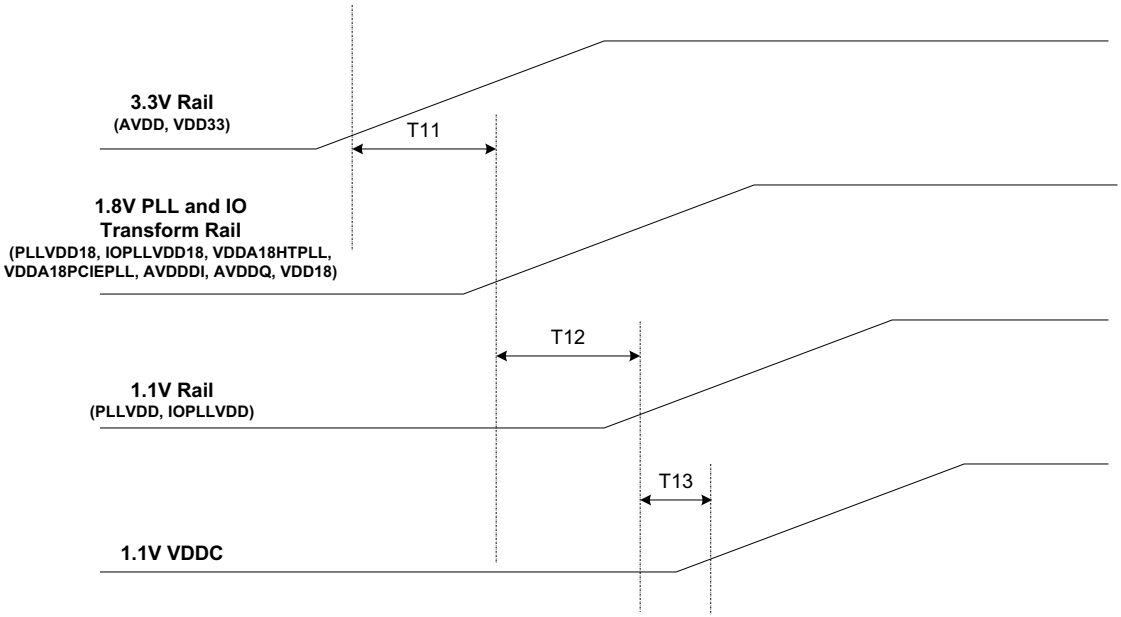
11 Defined as $t_{HIGH}/t_{CYCLE}$.

## 4.3 PCI Express® Differential Clock AC Specifications

**Table 4-2 PCI Express® Differential Clock (GFX_REFCLK, GPPSB_REFCLK, 100MHz) AC Characteristics**

| Symbol | Description | Minimum | Maximum | Unit |
|---|---|---|---|---|
| Rising Edge Rate | Rising Edge Rate | 0.6 | 4.0 | V/ns |
| Falling Edge Rate | Falling Edge Rate | 0.6 | 4.0 | V/ns |
| $T_{PERIOD\ AVG}$ | Average Clock Period Aquaria | -300 | +2800 | ppm |
| $T_{PERIOD\ ABS}$ | Absolute Period (including jitter and spread spectrum modulation) | 9.847 | 10.203 | ns |
| $T_{CCJITTER}$ | Cycle to Cycle Jitter | - | 150 | Ps |
| Duty Cycle | Duty Cycle | 40 | 60 | % |
| Rise-Fall Matching | Rising edge rate (REFCLK+) to falling edge rate (REFCLK-) matching | - | 20 | % |

## 4.4 Power Rail Power-up Sequence




Note: There are no specific requirements for the following 1.1V or 1.2V rails: VDDHT, VDDHTRX, VDDHTTX, VDDPCIE

**Figure 4-1 RX881 Power Rail Power-up Sequence**

**Table 4-3 RX881 Power Rail Power-up Sequence**

| Symbol | Parameter | Voltage Difference During Ramping | |
|---|---|---|---|
| | | Minimum (V) | Maximum (V) |
| T11 | 3.3-V rail ramps high relative to 1.8-V PLL and IO transform rails | 0 | 2.1 |
| T12 | 1.8-V PLL and IO transform rails ramp high relative to 1.1-V rail (PLLVDD, IOPLLVDD) | 0 | No restrictions |
| T13 | 1.1-V rail (PLLVDD, IOPLLVDD) ramps high relative to VDDC (1.1V) | 0 | No restrictions |

# Chapter 5
# Electrical Characteristics and Physical Data

## 5.1 Electrical Characteristics

### 5.1.1 Maximum and Minimum Ratings

**Table 5-1 Maximum and Minimum Ratings**

| Pin | Minimum | Typical | Maximum | Unit | Comments |
|---|---|---|---|---|---|
| VDDA18HTPLL | 1.71 | 1.8 | 1.89 | V | I/O power for HyperTransport™ PLL |
| VDDA18PCIE | 1.71 | 1.8 | 1.89 | V | 1.8V I/O power for PCIe® graphics, SB, and GPP interfaces |
| VDDA18PCIEPLL | 1.71 | 1.8 | 1.89 | V | 1.8V I/O power for PCIe PLLs |
| VDDC | 1.045 | 1.1 | 1.155 | V | Core power |
| VDD18 | 1.71 | 1.8 | 1.89 | V | 1.8V I/O transform power |
| VDD33 | 3.135 | 3.3 | 3.465 | V | 3.3V I/O power |
| VDDHT | 1.045 | 1.1 | 1.155 | V | I/O power for HyperTransport interface |
| VDDHTRX | 1.045 | 1.1 | 1.155 | V | I/O power for HyperTransport receive interface |
| VDDHTTX | 1.14 | 1.2 | 1.26 | V | I/O power for HyperTransport transmit interface |
| VDDPCIE | 1.045 | 1.1 | 1.155 | V | Main I/O power for PCIe graphics, SB, and GPP interfaces |

**Note:** Numbers in this table are to be qualified.

### 5.1.2 DC Characteristics

**Table 5-2 DC Characteristics for 3.3V TTL Signals**

| Pins | Symbol | Description | Minimum | Maximum | Unit |
|---|---|---|---|---|---|
| All pins belonging to the VDD33 domain (refer to pin description tables in this chapter). | VILdc | DC voltage at the pad that will produce a stable low input to the chip | – | 0.7 | V |
| | VIHdc | DC voltage at pad that will produce a stable high input to the chip | 1.4 | – | V |
| | VILac | AC input low voltage | – | 0.15 | V |
| | VIHac | AC input high voltage | 2.5 | – | V |
| | VOLdc | Output low voltage** | – | 0.53 | V |
| | VOHdc | Output high voltage** | 2.46 | – | V |
| | IOLdc | Output low current at V=0.1V** | 2.8 | – | mA |
| | IOHdc | Output high current at V=VDD33-0.1V** | 2.6 | – | mA |

**Note: *** Measured with edge rate of 1μs at PAD pin.
** For detailed current/voltage characteristics, please refer to the IBIS model.

**Table 5-3 DC Characteristics for POWERGOOD**

| Symbol | Description | Minimum | Typical | Maximum |
|---|---|---|---|---|
| VIL | Input Low Voltage | 0 | 0V | 300mV |
| VIH | Input High Voltage | 1.62V | 1.8V | 1.98V |

**Table 5-4 DC Characteristics for HyperTransport™ and PCI-E Differential Clock (HT_REFCLK, GFX_REFCLK, GPPSB_REFCLK, 100MHz)**

| Symbol | Description | Minimum | Maximum | Unit |
|---|---|---|---|---|
| $V_{IL}$ | Differential Input Low Voltage | - | -150 | mV |
| $V_{IH}$ | Differential Input High Voltage | +150 | - | mV |
| $V_{CROSS}$ | Absolute Crossing Point Voltage | +250 | +550 | mV |
| $V_{CROSS\ DELTA}$ | Variation of $V_{CROSS}$ over all rising clock edges | - | +140 | mV |
| $V_{RB}$ | Ring-back Voltage Margin | -100 | +100 | mV |
| $V_{IMAX}$ | Absolute Max Input Voltage | - | +1.15 | V |
| $V_{IMIN}$ | Absolute Min Input Voltage | - | -0.15 | V |

## 5.2 RX881 Thermal Characteristics

This section describes some key thermal parameters of the RX881. For a detailed discussion on these parameters and other thermal design descriptions including package level thermal data and analysis, please consult the *Thermal Design and Analysis Guidelines for the RS880 Product Family*, order# 46139.

### 5.2.1 RX881 Thermal Limits

**Table 5-5 RX881 Thermal Limits**

| Parameter | Minimum | Nominal | Maximum | Unit | Note |
|---|---|---|---|---|---|
| Operating Case Temperature | 0 | — | 95 | °C | 1 |
| Absolute Rated Junction Temperature | — | — | 115 | °C | 2 |
| Storage Temperature | -40 | — | 60 | °C | |
| Ambient Temperature | 0 | — | 45 | °C | 3 |
| Thermal Design Power | — | 11.4 | — | W | 4 |

**Notes:**
1 - The maximum operating case temperature is the die geometric top-center temperature measured via a thermocouple based on the methodology given in the document *Thermal Design and Analysis Guidelines for the RS880 Product Family*, order# 46139 (Chapter 12). This is the temperature at which the functionality of the chip is qualified.
2 - The maximum absolute rated junction temperature is the junction temperature at which the device can operate without causing damage to the ASIC. This temperature can be measured via the integrated thermal diode described in the next section.
3 - The ambient temperature is defined as the temperature of the local intake air to the thermal management device. The maximum ambient temperature is dependent on the heat sink's local ambient conditions as well as the chassis' external ambient, and the value given here is based on AMD's reference heat sink solution for the RX881. Refer to Chapter 6 in the *Thermal Design and Analysis Guidelines for the RS880 Product Family*, order# 46139 for heatsink and thermal design guidelines. Refer to Chapter 7 of the above mentioned document for details of ambient conditions.
4 - Thermal Design Power (TDP) is defined as the highest power dissipated while running currently available worst case applications at nominal voltages. Since the core power of modern ASICs using 65nm and smaller process technology can vary significantly, parts specifically screened for higher core power were used for TDP measurement. **The TDP is intended only as a design reference.**

### 5.2.2 Thermal Diode Characteristics

The RX881 has an on-die thermal diode, with its positive and negative terminals connected to the THERMALDIODE_P and THERMALDIODE_N pins respectively. Combined with a thermal sensor circuit, the diode temperature, and hence the ASIC temperature, can be derived from a differential voltage reading (*ΔV*). The equation relating *T* to *ΔV* is given below:

$$\Delta V = \frac{\eta \times K \times T \times \ln(N)}{q}$$

where:

*ΔV* = Difference of two base-to-emitter voltage readings, one using current = I and the other using current = *N x I*

*N* = Ratio of the two thermal diode currents (=10 when using an ADI thermal sensor, e.g. ADM 1020, 1030)

$\eta$ = Ideality factor of the diode

*K* = Boltzman's Constant

*T* = Temperature in Kelvin

*q* = Electron charge

The series resistance of the thermal diode ($R_T$) must be taken into account as it introduces an error in the reading (for every 1.0Ω, approximately $0.8^oC$ is added to the reading). The sensor circuit should be calibrated to offset the $R_T$ induced, plus any other known fixed error. Measured values of diode ideality factor and series resistance for the diode circuit are defined in the *Thermal Design and Analysis Guidelines for the RS880 Product Family*, order# 46139.

## 5.3 Package Information

### 5.3.1 Physical Dimensions

*Figure 5-1* and *Table 5-6* describe the physical dimensions of the RX881 package. *Figure 5-2* shows the detailed ball arrangement for the RX881.

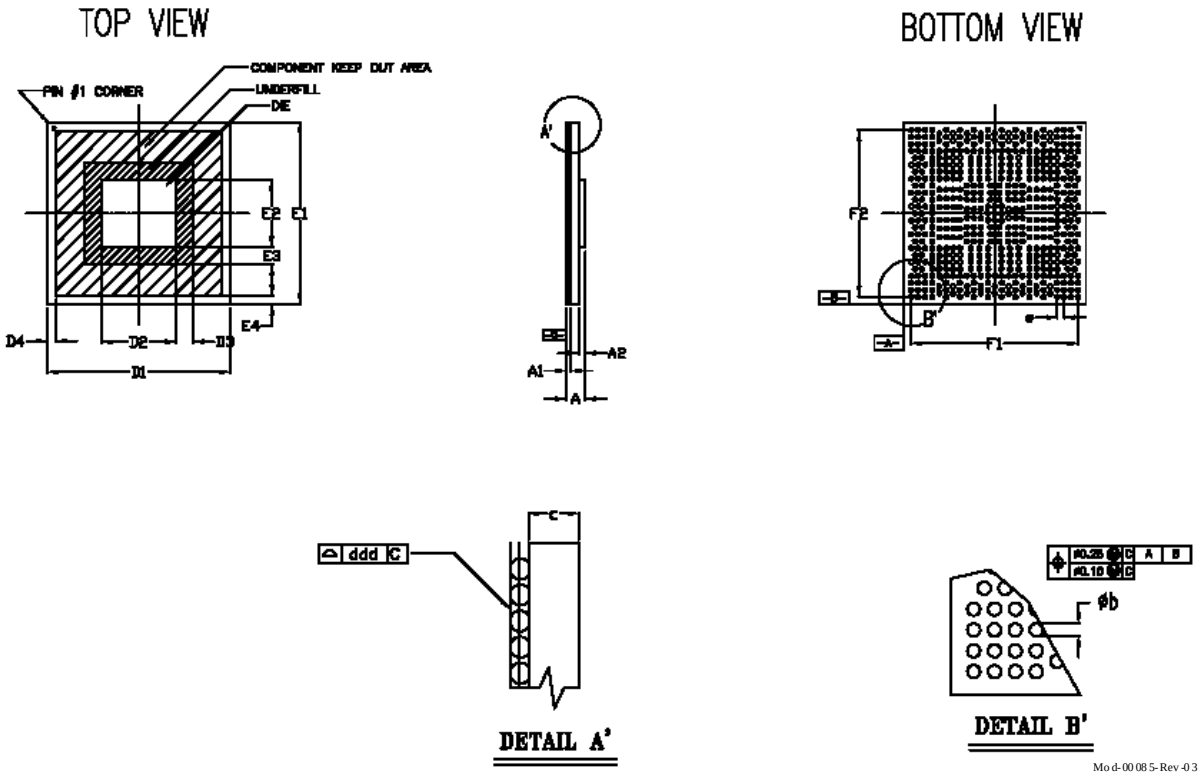



**Figure 5-1 RX881 528-Pin FCBGA Package Outline**

**Table 5-6 RX881 528-Pin FCBGA Package Physical Dimensions**

| Ref. | Min(mm) | Typical (mm) | Max. (mm) |
|---|---|---|---|
| c | 0.48 | 0.58 | 0.68 |
| A | 1.69 | 1.84 | 1.99 |
| A1 | 0.30 | 0.40 | 0.50 |
| A2 | 0.81 | 0.86 | 0.91 |
| ϕb | 0.40 | 0.50 | 0.60 |
| D1 | 20.85 | 21.00 | 21.15 |
| D2 | - | 8.58 | - |
| D3 | 2.00 | - | - |
| D4 | 1.00 | - | - |
| E1 | 20.85 | 21.00 | 21.15 |
| E2 | - | 7.70 | - |
| E3 | 2.00 | - | - |
| E4 | 1.00 | - | - |
| F1 | - | 19.20 | - |
| F2 | - | 19.20 | - |
| e1 | - | 0.80 (min. pitch) | - |
| ddd | - | - | 0.20 |

**Note**: Maximum height of SMT components is 0.650 mm.

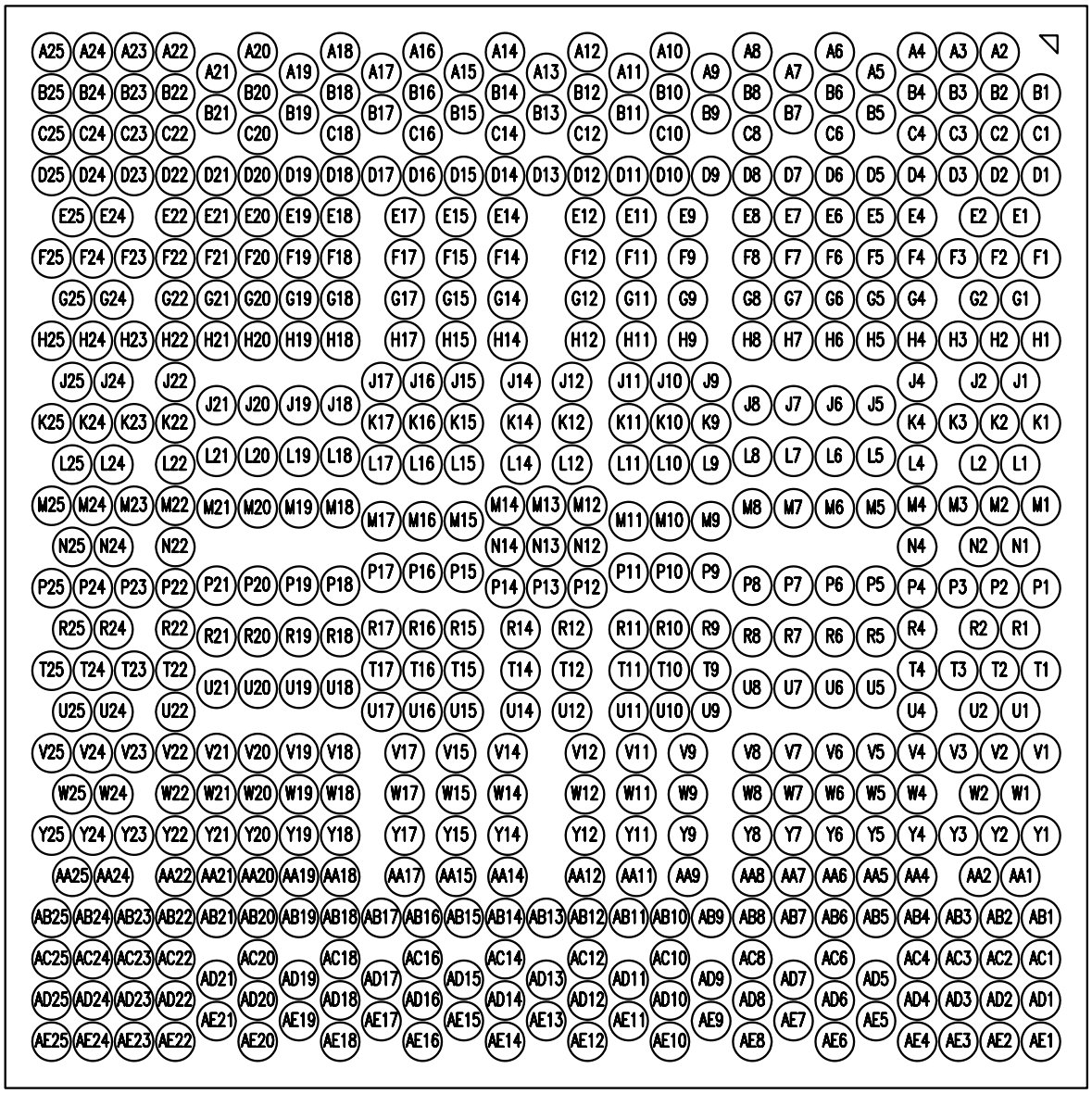



**Figure 5-2 RX881 Ball Arrangement (Bottom View)**

### 5.3.2 Pressure Specification

To avoid damages to the ASIC (die or solder ball joint cracks) caused by improper mechanical assembly of the cooling device, follow the recommendations below:

- It is recommended that the maximum load that is evenly applied across the contact area between the thermal management device and the die does not exceed 6 lbf. Note that a total load of 4-6 lbf is adequate to secure the thermal management device and achieve the lowest thermal contact resistance with a temperature drop across the thermal interface material of no more than 3°C. Also, the surface flatness of the metal spreader should be 0.001 inch/1 inch.
- Pre-test the assembly fixture with a strain gauge to make sure that the flexing of the final assembled board and the pressure applying around the ASIC package will not exceed 600 micron strain under any circumstances.
- Ensure that any distortion (bow or twist) of the board after SMT and cooling device assembly is within industry

guidelines (IPC/EIA J-STD-001). For measurement method, refer to the industry approved technique described in the manual IPC-TM-650, section 2.4.22.

### 5.3.3 Board Solder Reflow Process Recommendations

#### 5.3.3.1 Stencil Opening Size for Solder Paste Pads on PCB

It is recommended that the stencil aperture for solder paste be kept at the same size as that of the land pads. However, for the nine (or eight) pads at each corner of the ASIC package, the size of the openings should not exceed 400µm (see *Figure 5-3* below). This recommendation is based on AMD's sample land pattern design for the RX881, which is available from your AMD CSS representative.

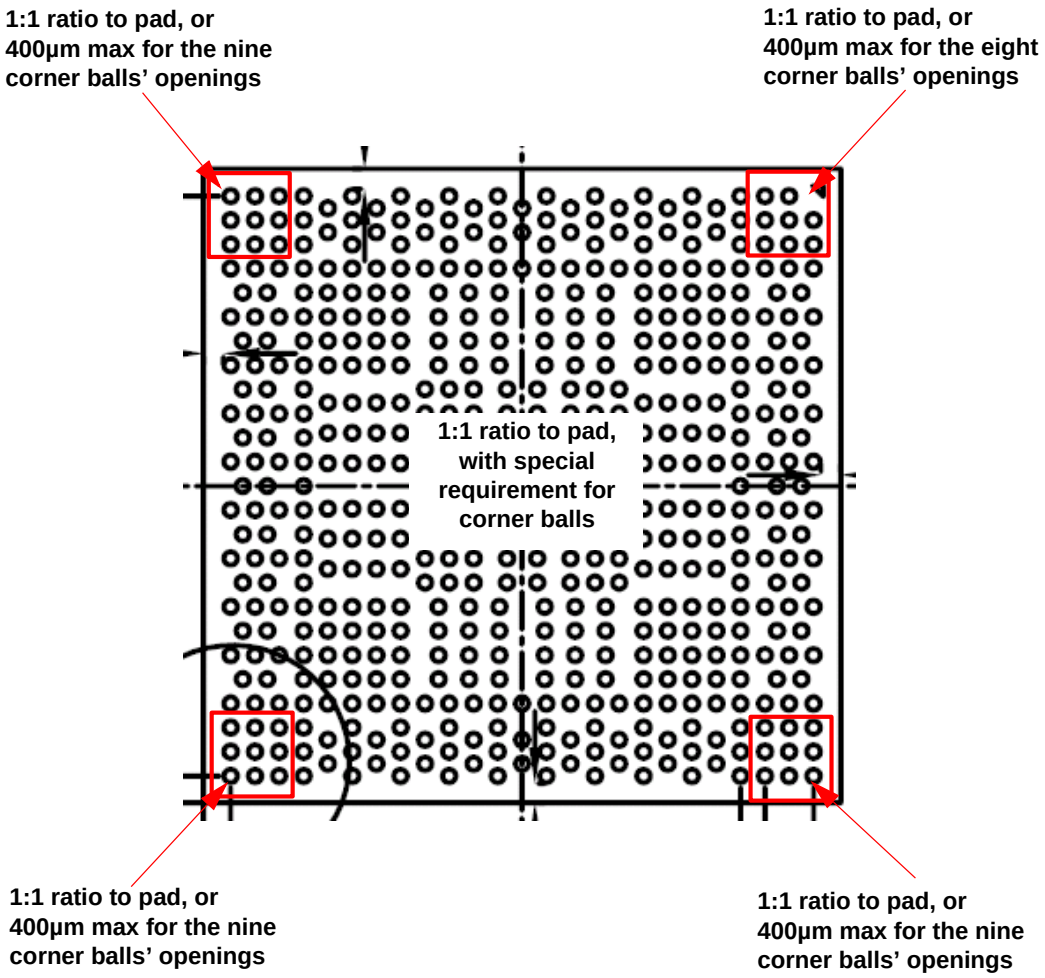



**Figure 5-3 Recommended Stencil Opening Sizes for Solder Paste Pads on PCB**

#### 5.3.3.2 Reflow Profile

A reference reflow profile is given below. Please note the following when using RoHS/lead-free solder (SAC105/305/405 Tin-Silver-Cu):

- The final reflow temperature profile will depend on the type of solder paste and chemistry of flux used in the SMT process. Modifications to the reference reflow profile may be required in order to accommodate the requirements of the other components in the application.
- An oven with 10 heating zones or above is recommended.
- To ensure that the reflow profile meets the target specification on both sides of the board, a different profile and oven recipe for the first and second reflow may be required.

- Mechanical stiffening can be used to minimize board warpage during reflow.
- It is suggested to decrease temperature cooling rate to minimize board warpage.
- This reflow profile applies only to RoHS/lead-free (high temperature) soldering process and it should not be used for Eutectic solder packages. Damage may result if this condition is violated.
- Maximum 3 reflows are allowed on the same part.

**Table 5-7 Recommended Board Solder Reflow Profile - RoHS/Lead-Free Solder**

| Profiling Stage | Temperature | Process Range |
|---|---|---|
| Overall Preheat | Room temp to 220°C | 2 mins to 4 mins |
| Soaking Time | 130°C to 170°C | Typical 60 – 80 seconds |
| Liquidus | 220°C | Typical 60 – 80 seconds |
| Ramp Rate | Ramp up and Cooling | <2°C / second |
| Peak | Max. 245°C | 235°C +/-5°C |
| Temperature at peak within 5°C | 240°C to 245°C | 10 – 30 seconds |

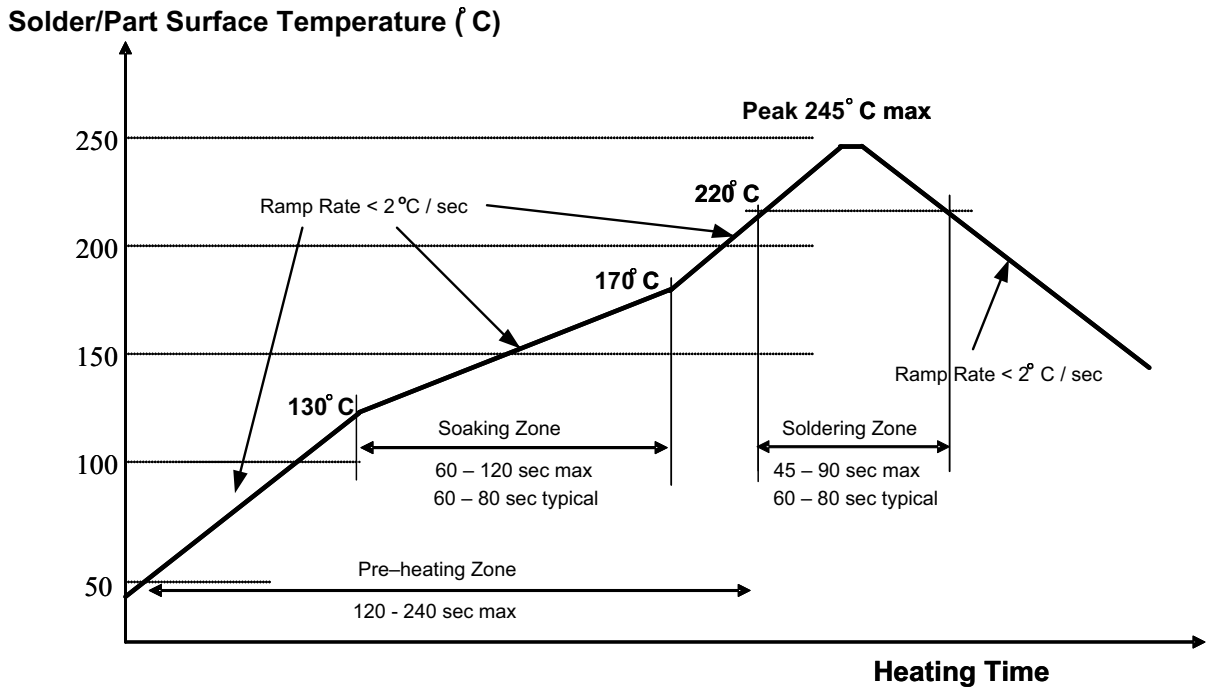



**Figure 5-4 RoHS/Lead-Free Solder (SAC305/405 Tin-Silver-Copper) Reflow Profile**

# Chapter 6
# Power Management and ACPI

## 6.1 ACPI Power Management Implementation

This chapter describes the support for ACPI power management provided by the RX881. The RX881 Northbridge supports ACPI Revision 2.0. The hardware, system BIOS, video BIOS, and drivers of the RX881 have all the logic required for meeting the power management specifications of PC2001, OnNow, and the Windows Logo Program and Device Requirements version 2.1. *Table 6-1, "ACPI States Supported by the RX881,"* describes the ACPI states supported by the RX881. *Table 6-2, "ACPI Signal Definitions,"* describes the signals used in the ACPI power management scheme of the RX881.

**Table 6-1 ACPI States Supported by the RX881**

| ACPI State | Description |
|---|---|
| Processor States: | |
| S0/C0: Working State | Working State. The processor is executing instructions. |
| S0/C1: Halt | CPU Halt state. No instructions are executed. This state has the lowest latency on resume and contributes minimum power savings. |
| S0/C2: Stop Grant Caches Snoopable | Stop Grant or Cache Snoopable CPU state. This state offers more power savings but has a higher latency on resume than the C1 state. |
| S0/C3/C1e: Stop Grant Caches Snoopable | Processor is put into Stop Grant state. Caches are still snoopable. The HyperTransport™ link may be disconnected and put into a low power state. System memory may be put into self-refresh. |
| System States: | |
| S3: Standby Suspend to RAM | System is off but context is saved to RAM. OEM support of this state is optional. System memory is put into self-refresh. |
| S4: Hibernate Suspend to Disk | System is off but context is saved to disk. When the system transitions to the working state, the OS is resumed without a system re-boot. |
| S5: Soft Off | System is off. OS re-boots when the system transitions to the working state. |
| G3: Mechanical Off | Occurs when system power (AC or battery) is not present or is unable to keep the system in one of the other states. |

**Note:** Also supported are additional processor power states that are not part of the ACPI specification, e.g. C1E (C1 Enhanced) and C3 pop-up. Please refer to the  and the *RS880 ASIC Family Register Programming Requirements*, order# 46141, for more information.

**Table 6-2 ACPI Signal Definitions**

| Signal Name | Description | Source |
|---|---|---|
| ALLOW_LDTSTOP | Output to the Southbridge to allow LDTSTOP# assertion. | Northbridge |
| LDTSTOP# | HyperTransport™ Technology Stop: Enables and disables links during system state transitions. | Southbridge |
| POWERON# | Power On | Power switch |
| RESET# | Global Reset | Southbridge |

**Figure 6-1 Linked List for Capabilities**

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# Chapter 7
# Testability

## 7.1 Test Capability Features

The RX881 has integrated test modes and capabilities. These test features cover both the ASIC and board level testing. The ASIC tests provide a very high fault coverage and low DPM (Defect Per Million) ratio of the part. The board level tests modes can be used for motherboard manufacturing and debug purposes. The following are the test modes of the RX881:

- Full scan implementation on the digital core logic that provides about 99% fault coverage through ATPG (Automatic Test Pattern Generation Vectors).
- Dedicated test logic for the on-chip custom memory macros to provide complete coverage on these modules.
- Improved access to the analog modules and PLLs in the RX881 to allow full evaluation and characterization of these modules.
- A JTAG test mode (which is not entirely compliant to the IEEE 1149.1 standard) to allow board level testing of neighboring devices.
- An XOR TREE test mode on all the digital I/O's to allow for proper soldering verification at the board level.
- A VOH/VOL test mode on all digital I/O's to allow for proper verification of output high and output low voltages at the board level.

These test modes can be accessed through the settings on the instruction register of the JTAG circuitry.

## 7.2 Test Interface

**Table 7-1 Pins on the Test Interface**

| Pin Name | Ball number | Type | Description |
|---|---|---|---|
| TESTMODE | D13 | I | IEEE 1149.1 test port reset |
| NC | B8 | I | TMS: Test Mode Select (IEEE 1149.1 test mode select) |
| NC | A9 | I | TDI: Test Mode Data In (IEEE 1149.1 data in) |
| NC | B9 | I | TCLK: Test Mode Clock (IEEE 1149.1 clock) |
| NC | D9 | O | TDO: Test Mode Data Out (IEEE 1149.1 data out) |
| POWERGOOD | A10 | I | I/O Reset |

## 7.3 XOR Test

### 7.3.1 Description of a Generic XOR Tree

An example of a generic XOR tree is shown in the *Figure 7-1*.

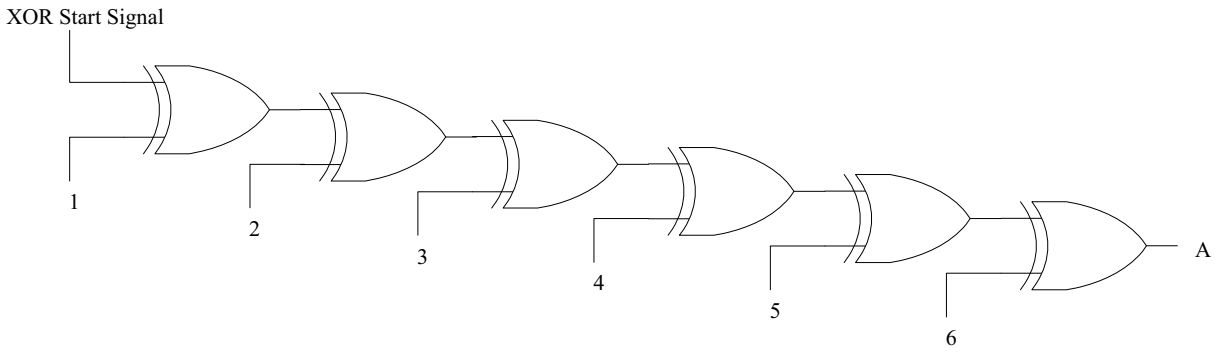


**Figure 7-1 Example of a Generic XOR Tree**

Pin A is assigned to the output direction, and pins 1 through 6 are assigned to the input direction. It can be seen that after all pins 1 to 6 are assigned to logic 0 or 1, a logic change in any one of these pins will toggle the output pin A.

The following is the truth table for the XOR tree shown in *Figure 7-1* The XOR start signal is assumed to be logic 1.

**Table 7-2 Example of an XOR Tree**

| Test Vector number | Input Pin 1 | Input Pin 2 | Input Pin 3 | Input Pin 4 | Input Pin 5 | Input Pin 6 | Output Pin A |
|---|---|---|---|---|---|---|---|
| 1 | 0 | 0 | 0 | 0 | 0 | 0 | 1 |
| 2 | 1 | 0 | 0 | 0 | 0 | 0 | 0 |
| 3 | 1 | 1 | 0 | 0 | 0 | 0 | 1 |
| 4 | 1 | 1 | 1 | 0 | 0 | 0 | 0 |
| 5 | 1 | 1 | 1 | 1 | 0 | 0 | 1 |
| 6 | 1 | 1 | 1 | 1 | 1 | 0 | 0 |
| 7 | 1 | 1 | 1 | 1 | 1 | 1 | 1 |

### 7.3.2 Description of the RX881 XOR Tree

### 7.3.3 XOR Tree Activation

The RX881 chip enters the XOR tree test mode by means of the JTAG. First, the 8-bit instruction register of the JTAG is loaded with the XOR instruction (“00001000”). This instruction assigns the input direction to all the pins except pin TDO, which is assigned the output direction to serve as the output of the XOR tree. After loading, the JTAG is taken to the Run-Test state for completion of the XOR tree initialization.

A 10MHz clock frequency for the Test Mode Clock (I2C_CLK) is recommended for the XOR TREE test mode. A pair of differential clock at 10MHz should also be supplied to HT_REFCLKP/N to enable I/Os for testing.

### 7.3.4 XOR Tree for the RX881

The XOR start signal is applied at the TDI Pin of the JTAG circuitry and the output of the XOR tree is obtained at the TDO Pin. Refer to *Table 7-3* for the list of the signals included on the XOR tree. A toggle of any of these balls in the XOR tree will cause the output to toggle.

There is no specific connection order to the signals on the tree. When the XOR tree is activated, any pin on the XOR tree must be either pulled down or pulled up to the I/O voltage of the pin. Only pins that are **not** on the XOR tree can be left floating.

When differential signal pairs are listed as single entries on the XOR tree, opposite input values should be applied to the two signals in each pair (e.g., for entry no. 1 on the tree, when “1” is applied to HT_RXCAD0P, “0” should be applied to HT_RXCAD0N).

**Table 7-3 RX881 XOR Tree**

| No. | Pin Name | Ball Reference |
|---|---|---|
| 1 | HT_RXCAD0P/N | Y25/Y24 |
| 2 | HT_RXCAD1P/N | V22/V23 |
| 3 | HT_RXCAD2P/N | V25/V24 |
| 4 | HT_RXCAD3P/N | U24/U25 |
| 5 | HT_RXCAD4P/N | T25/T24 |
| 6 | HT_RXCAD5P/N | P22/P23 |
| 7 | HT_RXCAD6P/N | P25/P24 |
| 8 | HT_RXCAD7P/N | N24/N25 |
| 9 | HT_RXCAD8P/N | AC24/AC25 |
| 10 | HT_RXCAD9P/N | AB25/AB24 |
| 11 | HT_RXCAD10P/N | AA24/AA25 |
| 12 | HT_RXCAD11P/N | Y22/Y23 |
| 13 | HT_RXCAD12P/N | W21/W20 |
| 14 | HT_RXCAD13P/N | V21/V20 |
| 15 | HT_RXCAD14P/N | U20/U21 |
| 16 | HT_RXCAD15P/N | U19/U18 |
| 17 | HT_RXCTL0P/N | M22/M23 |
| 18 | HT_RXCTL1P/N | R21/R20 |
| 19 | NC | AB18 |
| 20 | NC | AB13 |
| 21 | NC | V14 |
| 22 | NC | AD18 |
| 23 | NC | W12 |
| 24 | NC | Y12 |
| 25 | NC | AD16 |
| 26 | NC | AE17 |
| 27 | NC | AD17 |
| 28 | NC | AB12 |
| 29 | NC | AE16 |
| 30 | NC | V11 |
| 31 | NC | AE15 |
| 32 | NC | AA12 |
| 33 | NC | AB16 |
| 34 | NC | AB14 |
| 35 | NC | AD14 |
| 36 | NC | AD13 |
| 37 | NC | AD15 |
| 38 | NC | AC16 |
| 39 | NC | AE13 |
| 40 | NC | AC14 |
| 41 | NC | Y14 |
| 42 | NC | AA18 |
| 43 | NC | AA20 |
| 44 | NC | AA19 |
| 45 | NC | Y19 |
| 46 | NC | V17 |
| 47 | NC | AA17 |
| 48 | NC | AA15 |
| 49 | NC | Y15 |
| 50 | NC | AC20 |
| 51 | NC | AD19 |
| 52 | NC | AE22 |
| 53 | NC | AC18 |
| 54 | NC | AB20 |
| 55 | NC | AD22 |
| 56 | NC | AC22 |
| 57 | NC | AD21 |
| 58 | NC | W17 |
| 59 | NC | AE19 |
| 60 | NC/NC | Y17/W18 |
| 61 | NC/NC | AD20/AE21 |
| 62 | NC/NC | V15/W14 |
| 63 | GFX_RX0P/N | D4/C4 |
| 64 | GFX_RX1P/N | A3/B3 |
| 65 | GFX_RX2P/N | C2/C1 |
| 66 | GFX_RX3P/N | E5/F5 |
| 67 | GFX_RX4P/N | G5/G6 |
| 68 | GFX_RX5P/N | H5/H6 |
| 69 | GFX_RX6P/N | J6/J5 |
| 70 | GFX_RX7P/N | J7/J8 |

| No. | Pin Name | Ball Reference |
|---|---|---|
| 71 | GFX_RX8P/N | L5/L6 |
| 72 | GFX_RX9P/N | M8/L8 |
| 73 | GFX_RX10P/N | P7/M7 |
| 74 | GFX_RX11P/N | P5/M5 |
| 75 | GFX_RX12P/N | R8/P8 |
| 76 | GFX_RX13P/N | R6/R5 |
| 77 | GFX_RX14P/N | P4/P3 |
| 78 | GFX_RX15P/N | T4/T3 |
| 79 | GPP_RX0P/N | AE3/AD4 |
| 80 | GPP_RX1P/N | AE2/AD3 |
| 81 | GPP_RX2P/N | AD1/AD2 |
| 82 | GPP_RX3P/N | V5/W6 |
| 83 | GPP_RX4P/N | U5/U6 |
| 84 | GPP_RX5P/N | U8/U7 |
| 85 | SB_RX0P/N | AA8/Y8 |
| 86 | SB_RX1P/N | AA7/Y7 |
| 87 | SB_RX2P/N | AA5/AA6 |
| 88 | SB_RX3P/N | W5/Y5 |
| 89 | GPIO3 | E9 |
| 90 | GPIO4 | G12 |
| 91 | GPIO2 | F7 |
| 92 | DAC_HSYNC | A11 |
| 93 | DAC_VSYNC | B11 |
| 94 | NC | F8 |
| 95 | NC | A8 |
| 96 | NC | D10 |
| 97 | NC | A7 |
| 98 | NC | B7 |

## 7.4 VOH/VOL Test

### 7.4.1 Description of a Generic VOH/VOL Tree

The VOH/VOL logic gives signal output on I/O's when test patterns are applied through the TEST_ODD and TEST_EVEN inputs. Sample of a generic VOH/VOL tree is shown in *Figure 7-2*.

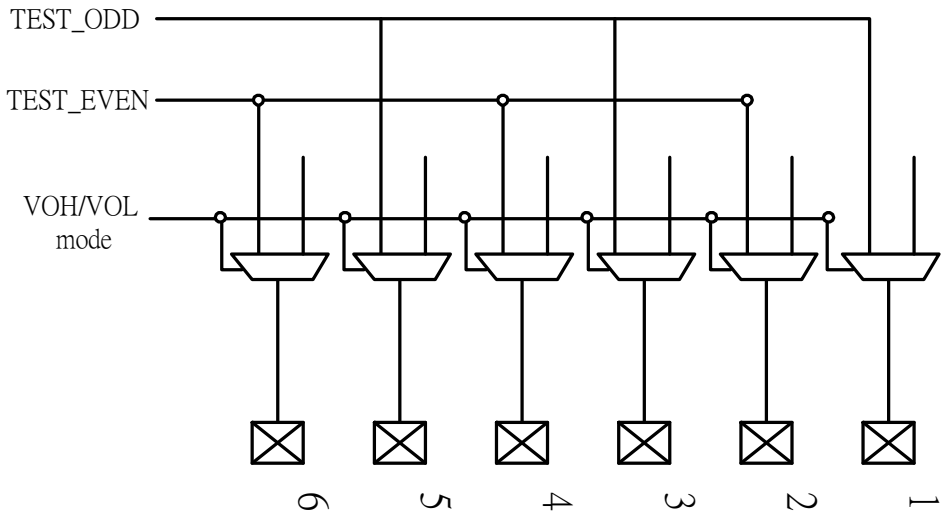


**Figure 7-2 Sample of a Generic VOH/VOL Tree**

The following is the truth table for the above VOH/VOL tree.

**Table 7-4 Truth Table for the VOH/VOL Tree Outputs**

| Test Vector Number | TEST_ODD Input | TEST_EVEN Input | Output Pin 1 | Output Pin 2 | Output Pin 3 | Output Pin 4 | Output Pin 5 | Output Pin 6 |
|---|---|---|---|---|---|---|---|---|
| 1 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 |
| 2 | 0 | 1 | 0 | 1 | 0 | 1 | 0 | 1 |
| 3 | 1 | 0 | 1 | 0 | 1 | 0 | 1 | 0 |
| 4 | 1 | 1 | 1 | 1 | 1 | 1 | 1 | 1 |

Refer to *Section 7.4.3* for the list of pins that are on the VOH/VOL tree. VOH/VOL Tree Activation

### 7.4.2 VOH/VOL Tree Activation

To activate the VOH/VOL tree and run a VOH/VOL test, perform the sequence below:

1. Supply a 10MHz clock to the REFCLK_P pin and a 10MHz differential clock pair to the HT_REFCLKP/N pins to enable I/Os for testing.

2. Set POWERGOOD to 0.

3. Set TESTMODE to 1.

4. Set NC (ball E8) to 0.

5. Load JTAG instruction register with the instruction 0110 0011.

6. Load JTAG instruction register with the instruction 0010 0111.

7. Set POWERGOOD to 1.

8. Load JTAG instruction register with the instruction 1001 1001.

9. Run test by loading JTAG data register with data 0000 0000 0000 00xy, where bit x is the input value for TEST_ODD and bit y that for TEST_EVEN (see Table 7-4 above).

10. To end test, load JTAG instruction register with the instruction 0101 1101.

### 7.4.3 VOH/VOL Pin List

Table 7-5 shows the RX881 VOH/VOL tree. There is no specific order for connection. Under the Control column, an "ODD" or "EVEN" indicates that the logical output of the pin is same as the "TEST_ODD" or "TEST_EVEN" input respectively.

When a differential pair appear in the table as a single entry, the output of the positive ("P") pin is indicated in the Control column (see last paragraph for explanations), and the output of the negative pin ("N") will be of the opposite value. For example, for entry no. 1 on the tree, when TEST_EVEN is 1, HT_TXCAD0P will give a value of 1 and HT_TXCAD0N will give a value of 0.

**Table 7-5 RX881 VOH/VOL Tree**

| No. | Pin Name | Ball Reference | Control |
|---|---|---|---|
| 1 | HT_TXCAD0P/N | D24/D25 | Even |
| 2 | HT_TXCAD1P/N | E24/E25 | Odd |
| 3 | HT_TXCAD2P/N | F24/F25 | Even |
| 4 | HT_TXCAD3P/N | F23/F22 | Odd |
| 5 | HT_TXCAD4P/N | H23/H22 | Even |
| 6 | HT_TXCAD5P/N | J25/J24 | Odd |
| 7 | HT_TXCAD6P/N | K24/K25 | Even |
| 8 | HT_TXCAD7P/N | K23/K22 | Odd |
| 9 | HT_TXCAD8P/N | F21/G21 | Even |
| 10 | HT_TXCAD9P/N | G20/H21 | Odd |
| 11 | HT_TXCAD10P/N | J20/J21 | Even |
| 12 | HT_TXCAD11P/N | J18/K17 | Odd |
| 13 | HT_TXCAD12P/N | L19/J19 | Even |
| 14 | HT_TXCAD13P/N | M19/L18 | Odd |
| 15 | HT_TXCAD14P/N | M21/P21 | Even |
| 16 | HT_TXCAD15P/N | P18/M18 | Odd |
| 17 | HT_TXCTL0P/N | M24/M25 | Even |
| 18 | HT_TXCTL1P/N | P19/R18 | Odd |
| 19 | NC | AA18 | Even |
| 20 | NC | AA20 | Odd |
| 21 | NC | AA19 | Even |
| 22 | NC | Y19 | Odd |
| 23 | NC | V17 | Even |
| 24 | NC | AA17 | Odd |
| 25 | NC | AA15 | Even |
| 26 | NC | Y15 | Odd |
| 27 | NC | AC20 | Even |
| 28 | NC | AD19 | Odd |
| 29 | NC | AE22 | Even |
| 30 | NC | AC18 | Odd |
| 31 | NC | AB20 | Even |
| 32 | NC | AD22 | Odd |
| 33 | NC | AC22 | Even |
| 34 | NC | AD21 | Odd |
| 35 | NC | W17 | Even |
| 36 | NC | AE19 | Odd |
| 37 | NC/NC | Y17/W18 | Even |
| 38 | NC/NC | AD20/AE21 | Odd |
| 39 | NC | AB18 | Even |
| 40 | NC | AB13 | Odd |
| 41 | NC | V14 | Even |
| 42 | NC | AD18 | Odd |
| 43 | NC | W12 | Even |
| 44 | NC | Y12 | Odd |
| 45 | NC | AD16 | Even |
| 46 | NC | AE17 | Odd |
| 47 | NC | AD17 | Even |
| 48 | NC | AB12 | Odd |
| 49 | NC | AE16 | Even |
| 50 | NC | V11 | Odd |
| 51 | NC | AE15 | Even |
| 52 | NC | AA12 | Odd |
| 53 | NC | AB16 | Even |
| 54 | NC | AB14 | Odd |
| 55 | NC | AD14 | Even |
| 56 | NC | AD13 | Odd |
| 57 | NC | AD15 | Even |
| 58 | NC | AC16 | Odd |
| 59 | NC | AE13 | Even |
| 60 | NC | AC14 | Odd |
| 61 | NC | Y14 | Even |
| 62 | NC/NC | V15/W14 | Odd |
| 63 | GFX_TX0P/N | A5/B5 | Even |
| 64 | GFX_TX1P/N | A4/B4 | Odd |
| 65 | GFX_TX2P/N | C3/B2 | Even |
| 66 | GFX_TX3P/N | D1/D2 | Odd |
| 67 | GFX_TX4P/N | E2/E1 | Even |
| 68 | GFX_TX5P/N | F4/F3 | Odd |
| 69 | GFX_TX6P/N | F1/F2 | Even |
| 70 | GFX_TX7P/N | H4/H3 | Odd |

| No. | Pin Name | Ball Reference | Control |
|---|---|---|---|
| 71 | GFX_TX8P/N | H1/H2 | Even |
| 72 | GFX_TX9P/N | J2/J1 | Odd |
| 73 | GFX_TX10P/N | K4/K3 | Even |
| 74 | GFX_TX11P/N | K1/K2 | Odd |
| 75 | GFX_TX12P/N | M4/M3 | Even |
| 76 | GFX_TX13P/N | M1/M2 | Odd |
| 77 | GFX_TX14P/N | N2/N1 | Even |
| 78 | GFX_TX15P/N | P1/P2 | Odd |
| 79 | GPP_TX0P/N | AC1/AC2 | Even |
| 80 | GPP_TX1P/N | AB4/AB3 | Odd |
| 81 | GPP_TX2P/N | AA2/AA1 | Even |
| 82 | GPP_TX3P/N | Y1/Y2 | Odd |
| 83 | GPP_TX4P/N | Y4/Y3 | Even |
| 84 | GPP_TX5P/N | V1/V2 | Odd |
| 85 | SB_TX0P/N | AD7/AE7 | Even |
| 86 | SB_TX1P/N | AE6/AD6 | Odd |
| 87 | SB_TX2P/N | AB6/AC6 | Even |
| 88 | SB_TX3P/N | AD5/AE5 | Odd |
| 89 | GPIO2 | F7 | Even |
| 90 | GPIO4 | G12 | Odd |
| 91 | GPIO3 | E9 | Even |
| 92 | DAC_VSYNC | B11 | Odd |
| 93 | DAC_HSYNC | A11 | Even |
| 94 | NC | D10 | Odd |

# Appendix A
## *Pin Listings*

This appendix contains pin listings for the RX881 sorted in different ways. To go to the listing of interest, use the linked cross-references below:

*"RX881 Pin List Sorted by Ball Reference" on page A-2*

*"RX881 Pin List Sorted by Pin Name" on page A-7*

## A.1 RX881 Pin List Sorted by Ball Reference

**Table A-1 RX881 Pin List Sorted by Ball Reference**

| Ball Ref | Pin Name |
|---|---|
| A10 | POWERGOOD |
| A11 | DAC_HSYNC |
| A12 | PLLVDD |
| A13 | VDDLTP18 |
| A14 | VDDLT33 |
| A15 | VDDLT18 |
| A16 | NC |
| A17 | NC |
| A18 | NC |
| A19 | NC |
| A2 | VSSAPCIE |
| A20 | NC |
| A21 | NC |
| A22 | NC |
| A23 | VDDHTRX |
| A24 | HT_RXCALN |
| A25 | VSSAHT |
| A3 | GFX_RX1P |
| A4 | GFX_TX1P |
| A5 | GFX_TX0P |
| A6 | VDDPCIE |
| A7 | NC |
| A8 | NC |
| A9 | NC |
| AA1 | GPP_TX2N |
| AA11 | VDD_MEM |
| AA12 | NC |
| AA14 | VSS |
| AA15 | NC |
| AA17 | NC |
| AA18 | NC |
| AA19 | NC |
| AA2 | GPP_TX2P |
| AA20 | NC |
| AA21 | VDDHTTX |
| AA22 | HT_RXCLK1N |
| AA24 | HT_RXCAD10P |
| AA25 | HT_RXCAD10N |
| AA4 | VSSAPCIE |
| AA5 | SB_RX2P |
| AA6 | SB_RX2N |
| AA7 | SB_RX1P |
| AA8 | SB_RX0P |
| AA9 | VDDA18PCIE |
| AB1 | VSSAPCIE |
| AB10 | VDD_MEM |
| AB11 | VSS |
| AB12 | NC |
| AB13 | NC |
| AB14 | NC |
| AB15 | VSS |
| AB16 | NC |
| AB17 | VSS |
| AB18 | NC |
| AB19 | VSS |
| AB2 | VSSAPCIE |
| AB20 | NC |
| AB21 | VSS |
| AB22 | VDDHTTX |
| AB23 | HT_RXCLK1P |
| AB24 | HT_RXCAD9N |
| AB25 | HT_RXCAD9P |
| AB3 | GPP_TX1N |
| AB4 | GPP_TX1P |
| AB5 | VSSAPCIE |
| AB6 | SB_TX2P |
| AB7 | VSSAPCIE |
| AB8 | PCE_CALRN |
| AB9 | VDDA18PCIE |
| AC1 | GPP_TX0P |
| AC10 | VDD_MEM |
| AC12 | VSS |
| AC14 | NC |
| AC16 | NC |
| AC18 | NC |
| AC2 | GPP_TX0N |
| AC20 | NC |
| AC22 | NC |
| AC23 | VDDHTTX |
| AC24 | HT_RXCAD8P |
| AC25 | HT_RXCAD8N |
| AC3 | VSSAPCIE |
| AC4 | VSSAPCIE |
| AC6 | SB_TX2N |
| AC8 | PCE_CALRP |
| AD1 | GPP_RX2P |
| AD10 | VDD_MEM |
| AD11 | VDD18_MEM |
| AD12 | NC |
| AD13 | NC |
| AD14 | NC |
| AD15 | NC |
| AD16 | NC |
| AD17 | NC |
| AD18 | NC |
| AD19 | NC |
| AD2 | GPP_RX2N |
| AD20 | NC |
| AD21 | NC |
| AD22 | NC |
| AD23 | IOPLLVSS |
| AD24 | VDDHTTX |
| AD25 | VSSAHT |
| AD3 | GPP_RX1N |
| AD4 | GPP_RX0N |
| AD5 | SB_TX3P |
| AD6 | SB_TX1N |
| AD7 | SB_TX0P |
| AD8 | THERMALDIODE_N |
| AD9 | VDDA18PCIE |
| AE1 | VSSAPCIE |
| AE10 | VDD_MEM |
| AE11 | VDD18_MEM |
| AE12 | NC |
| AE13 | NC |
| AE14 | VSS |
| AE15 | NC |
| AE16 | NC |
| AE17 | NC |
| AE18 | MEM_VREF |
| AE19 | NC |
| AE2 | GPP_RX1P |
| AE20 | VSS |
| AE21 | NC |
| AE22 | NC |
| AE23 | IOPLLVDD18 |

| Ball Ref | Pin Name |
|---|---|
| AE24 | IOPLLVDD |
| AE25 | VDDHTTX |
| AE3 | GPP_RX0P |
| AE4 | VSSAPCIE |
| AE5 | SB_TX3N |
| AE6 | SB_TX1P |
| AE7 | SB_TX0N |
| AE8 | THERMALDIODE_P |
| AE9 | VDDA18PCIE |
| B1 | VSSAPCIE |
| B10 | STRP_DATA |
| B11 | DAC_VSYNC |
| B12 | PLLVSS |
| B13 | VSSLTP18 |
| B14 | VDDLT33 |
| B15 | VDDLT18 |
| B16 | NC |
| B17 | NC |
| B18 | NC |
| B19 | NC |
| B2 | GFX_TX2N |
| B20 | NC |
| B21 | NC |
| B22 | NC |
| B23 | VDDHTRX |
| B24 | HT_TXCALP |
| B25 | HT_TXCALN |
| B3 | GFX_RX1N |
| B4 | GFX_TX1N |
| B5 | GFX_TX0N |
| B6 | VDDPCIE |
| B7 | NC |
| B8 | NC |
| B9 | NC |
| C1 | GFX_RX2N |
| C10 | LDTSTOP# |
| C12 | ALLOW_LDTSTOP |
| C14 | VSSLT |
| C16 | VSSLT |
| C18 | VSSLT |
| C2 | GFX_RX2P |
| C20 | VSSLT |
| C22 | VSSLT |
| C23 | HT_RXCALP |

| Ball Ref | Pin Name |
|---|---|
| C24 | HT_REFCLKN |
| C25 | HT_REFCLKP |
| C3 | GFX_TX2P |
| C4 | GFX_RX0N |
| C6 | VDDPCIE |
| C8 | NC |
| D1 | GFX_TX3P |
| D10 | NC |
| D11 | VSS |
| D12 | SUS_STAT# |
| D13 | TESTMODE |
| D14 | PLLVDD18 |
| D15 | VSSLT |
| D16 | NC |
| D17 | NC |
| D18 | NC |
| D19 | NC |
| D2 | GFX_TX3N |
| D20 | NC |
| D21 | NC |
| D22 | VDDHTRX |
| D23 | VSSAHT |
| D24 | HT_TXCAD0P |
| D25 | HT_TXCAD0N |
| D3 | VSSAPCIE |
| D4 | GFX_RX0P |
| D5 | VSSAPCIE |
| D6 | VDDPCIE |
| D7 | VDDA18PCIEPLL |
| D8 | SYSRESET# |
| D9 | NC |
| E1 | GFX_TX4N |
| E11 | REFCLK_P |
| E12 | AVDD |
| E14 | VSS |
| E15 | VSS |
| E17 | NC |
| E18 | NC |
| E19 | NC |
| E2 | GFX_TX4P |
| E20 | VSSLT |
| E21 | VDDHTRX |
| E22 | VSSAHT |
| E24 | HT_TXCAD1P |

| Ball Ref | Pin Name |
|---|---|
| E25 | HT_TXCAD1N |
| E4 | VSSAPCIE |
| E5 | GFX_RX3P |
| E6 | VDDPCIE |
| E7 | VDDA18PCIEPLL |
| E8 | NC |
| E9 | GPIO3 |
| F1 | GFX_TX6P |
| F11 | REFCLK_N |
| F12 | AVDD |
| F14 | AVDDDI |
| F15 | NC |
| F17 | NC |
| F18 | VSS |
| F19 | VSS |
| F2 | GFX_TX6N |
| F20 | VDDHTRX |
| F21 | HT_TXCAD8P |
| F22 | HT_TXCAD3N |
| F23 | HT_TXCAD3P |
| F24 | HT_TXCAD2P |
| F25 | HT_TXCAD2N |
| F3 | GFX_TX5N |
| F4 | GFX_TX5P |
| F5 | GFX_RX3N |
| F6 | VDDPCIE |
| F7 | GPIO2 |
| F8 | NC |
| F9 | VDD18 |
| G1 | VSSAPCIE |
| G11 | RESERVED |
| G12 | GPIO4 |
| G14 | NC |
| G15 | AVSSDI |
| G17 | VSS |
| G18 | NC |
| G19 | VDDHTRX |
| G2 | VSSAPCIE |
| G20 | HT_TXCAD9P |
| G21 | HT_TXCAD8N |
| G22 | VSSAHT |
| G24 | VSSAHT |
| G25 | VSSAHT |
| G4 | VSSAPCIE |

| Ball Ref | Pin Name |
|---|---|
| G5 | GFX_RX4P |
| G6 | GFX_RX4N |
| G7 | VDDPCIE |
| G8 | VSS |
| G9 | VDD18 |
| H1 | GFX_TX8P |
| H11 | VDD33 |
| H12 | VDD33 |
| H14 | AVSSQ |
| H15 | AVDDQ |
| H17 | VDDA18HTPLL |
| H18 | VDDHTRX |
| H19 | VSSAHT |
| H2 | GFX_TX8N |
| H20 | VSSAHT |
| H21 | HT_TXCAD9N |
| H22 | HT_TXCAD4N |
| H23 | HT_TXCAD4P |
| H24 | HT_TXCLK0P |
| H25 | HT_TXCLK0N |
| H3 | GFX_TX7N |
| H4 | GFX_TX7P |
| H5 | GFX_RX5P |
| H6 | GFX_RX5N |
| H7 | VSSAPCIE |
| H8 | VDDPCIE |
| H9 | VDDA18PCIE |
| J1 | GFX_TX9N |
| J10 | VDDA18PCIE |
| J11 | VDDC |
| J12 | VSS |
| J14 | VDDC |
| J15 | VSS |
| J16 | VDDC |
| J17 | VDDHT |
| J18 | HT_TXCAD11P |
| J19 | HT_TXCAD12N |
| J2 | GFX_TX9P |
| J20 | HT_TXCAD10P |
| J21 | HT_TXCAD10N |
| J22 | VSSAHT |
| J24 | HT_TXCAD5N |
| J25 | HT_TXCAD5P |
| J4 | VSSAPCIE |

| Ball Ref | Pin Name |
|---|---|
| J5 | GFX_RX6N |
| J6 | GFX_RX6P |
| J7 | GFX_RX7P |
| J8 | GFX_RX7N |
| J9 | VDDPCIE |
| K1 | GFX_TX11P |
| K10 | VDDA18PCIE |
| K11 | VSS |
| K12 | VDDC |
| K14 | VSS |
| K15 | VDDC |
| K16 | VDDHT |
| K17 | HT_TXCAD11N |
| K2 | GFX_TX11N |
| K22 | HT_TXCAD7N |
| K23 | HT_TXCAD7P |
| K24 | HT_TXCAD6P |
| K25 | HT_TXCAD6N |
| K3 | GFX_TX10N |
| K4 | GFX_TX10P |
| K9 | VDDPCIE |
| L1 | VSSAPCIE |
| L10 | VDDA18PCIE |
| L11 | VDDC |
| L12 | VSS |
| L14 | VDDC |
| L15 | VSS |
| L16 | VDDHT |
| L17 | VSSAHT |
| L18 | HT_TXCAD13N |
| L19 | HT_TXCAD12P |
| L2 | VSSAPCIE |
| L20 | HT_TXCLK1N |
| L21 | HT_TXCLK1P |
| L22 | VSSAHT |
| L24 | VSSAHT |
| L25 | VSSAHT |
| L4 | VSSAPCIE |
| L5 | GFX_RX8P |
| L6 | GFX_RX8N |
| L7 | VSSAPCIE |
| L8 | GFX_RX9N |
| L9 | VDDPCIE |
| M1 | GFX_TX13P |

| Ball Ref | Pin Name |
|---|---|
| M10 | VDDA18PCIE |
| M11 | VSS |
| M12 | VDDC |
| M13 | VDDC |
| M14 | VSS |
| M15 | VDDC |
| M16 | VDDHT |
| M17 | VDDHTTX |
| M18 | HT_TXCAD15N |
| M19 | HT_TXCAD13P |
| M2 | GFX_TX13N |
| M20 | VSSAHT |
| M21 | HT_TXCAD14P |
| M22 | HT_RXCTL0P |
| M23 | HT_RXCTL0N |
| M24 | HT_TXCTL0P |
| M25 | HT_TXCTL0N |
| M3 | GFX_TX12N |
| M4 | GFX_TX12P |
| M5 | GFX_RX11N |
| M6 | VSSAPCIE |
| M7 | GFX_RX10N |
| M8 | GFX_RX9P |
| M9 | VDDPCIE |
| N1 | GFX_TX14N |
| N12 | VDDC |
| N13 | VSS |
| N14 | VDDC |
| N2 | GFX_TX14P |
| N22 | VSSAHT |
| N24 | HT_RXCAD7P |
| N25 | HT_RXCAD7N |
| N4 | VSSAPCIE |
| P1 | GFX_TX15P |
| P10 | VDDA18PCIE |
| P11 | VDDC |
| P12 | VSS |
| P13 | VDDC |
| P14 | VDDC |
| P15 | VSS |
| P16 | VDDHT |
| P17 | VDDHTTX |
| P18 | HT_TXCAD15P |
| P19 | HT_TXCTL1P |

| Ball Ref | Pin Name |
|---|---|
| P2 | GFX_TX15N |
| P20 | VSSAHT |
| P21 | HT_TXCAD14N |
| P22 | HT_RXCAD5P |
| P23 | HT_RXCAD5N |
| P24 | HT_RXCAD6N |
| P25 | HT_RXCAD6P |
| P3 | GFX_RX14N |
| P4 | GFX_RX14P |
| P5 | GFX_RX11P |
| P6 | VSSAPCIE |
| P7 | GFX_RX10P |
| P8 | GFX_RX12N |
| P9 | VDDPCIE |
| R1 | VSSAPCIE |
| R10 | VDDA18PCIE |
| R11 | VSS |
| R12 | VDDC |
| R14 | VSS |
| R15 | VDDC |
| R16 | VDDHT |
| R17 | VDDHTTX |
| R18 | HT_TXCTL1N |
| R19 | VSSAHT |
| R2 | VSSAPCIE |
| R20 | HT_RXCTL1N |
| R21 | HT_RXCTL1P |
| R22 | VSSAHT |
| R24 | VSSAHT |
| R25 | VSSAHT |
| R4 | VSSAPCIE |
| R5 | GFX_RX13N |
| R6 | GFX_RX13P |
| R7 | VSSAPCIE |
| R8 | GFX_RX12P |
| R9 | VDDPCIE |
| T1 | GFX_REFCLKN |
| T10 | VDDA18PCIE |
| T11 | VDDC |
| T12 | VSS |
| T14 | VDDC |
| T15 | VDDC |
| T16 | VDDHT |
| T17 | VDDHTTX |

| Ball Ref | Pin Name |
|---|---|
| T2 | GFX_REFCLKP |
| T22 | HT_RXCLK0P |
| T23 | HT_RXCLK0N |
| T24 | HT_RXCAD4N |
| T25 | HT_RXCAD4P |
| T3 | GFX_RX15N |
| T4 | GFX_RX15P |
| T9 | VDDPCIE |
| U1 | GPP_REFCLKP |
| U10 | VDDA18PCIE |
| U11 | VSS |
| U12 | VDDC |
| U14 | VSS |
| U15 | VSS |
| U16 | VDDC |
| U17 | VDDHTTX |
| U18 | HT_RXCAD15N |
| U19 | HT_RXCAD15P |
| U2 | GPP_REFCLKN |
| U20 | HT_RXCAD14P |
| U21 | HT_RXCAD14N |
| U22 | VSSAHT |
| U24 | HT_RXCAD3P |
| U25 | HT_RXCAD3N |
| U4 | VSSAPCIE |
| U5 | GPP_RX4P |
| U6 | GPP_RX4N |
| U7 | GPP_RX5N |
| U8 | GPP_RX5P |
| U9 | VDDPCIE |
| V1 | GPP_TX5P |
| V11 | NC |
| V12 | VSS |
| V14 | NC |
| V15 | NC |
| V17 | NC |
| V18 | VDDHTTX |
| V19 | VSSAHT |
| V2 | GPP_TX5N |
| V20 | HT_RXCAD13N |
| V21 | HT_RXCAD13P |
| V22 | HT_RXCAD1P |
| V23 | HT_RXCAD1N |
| V24 | HT_RXCAD2N |

| Ball Ref | Pin Name |
|---|---|
| V25 | HT_RXCAD2P |
| V3 | GPPSB_REFCLKN |
| V4 | GPPSB_REFCLKP |
| V5 | GPP_RX3P |
| V6 | VSSAPCIE |
| V7 | VSSAPCIE |
| V8 | VSSAPCIE |
| V9 | VDDPCIE |
| W1 | VSSAPCIE |
| W11 | VSS |
| W12 | NC |
| W14 | NC |
| W15 | VSS |
| W17 | NC |
| W18 | NC |
| W19 | VDDHTTX |
| W2 | VSSAPCIE |
| W20 | HT_RXCAD12N |
| W21 | HT_RXCAD12P |
| W22 | VSSAHT |
| W24 | VSSAHT |
| W25 | VSSAHT |
| W4 | VSSAPCIE |
| W5 | SB_RX3P |
| W6 | GPP_RX3N |
| W7 | VSSAPCIE |
| W8 | VSSAPCIE |
| W9 | VDDA18PCIE |
| Y1 | GPP_TX3P |
| Y11 | VDD_MEM |
| Y12 | NC |
| Y14 | NC |
| Y15 | NC |
| Y17 | NC |
| Y18 | VSS |
| Y19 | NC |
| Y2 | GPP_TX3N |
| Y20 | VDDHTTX |
| Y21 | VSSAHT |
| Y22 | HT_RXCAD11P |
| Y23 | HT_RXCAD11N |
| Y24 | HT_RXCAD0N |
| Y25 | HT_RXCAD0P |
| Y3 | GPP_TX4N |

| Ball Ref | Pin Name |
|---|---|
| Y4 | GPP_TX4P |
| Y5 | SB_RX3N |
| Y6 | VSSAPCIE |
| Y7 | SB_RX1N |
| Y8 | SB_RX0N |
| Y9 | VDDA18PCIE |

## A.2 RX881 Pin List Sorted by Pin Name

**Table A-2 RX881 Pin List Sorted by Pin Name**

| Pin Name | Ball Ref |
|---|---|
| ALLOW_LDTSTOP | C12 |
| AVDD | E12 |
| AVDD | F12 |
| AVDDDI | F14 |
| AVDDQ | H15 |
| AVSSDI | G15 |
| AVSSQ | H14 |
| DAC_HSYNC | A11 |
| DAC_VSYNC | B11 |
| GFX_REFCLKN | T1 |
| GFX_REFCLKP | T2 |
| GFX_RX0N | C4 |
| GFX_RX0P | D4 |
| GFX_RX10N | M7 |
| GFX_RX10P | P7 |
| GFX_RX11N | M5 |
| GFX_RX11P | P5 |
| GFX_RX12N | P8 |
| GFX_RX12P | R8 |
| GFX_RX13N | R5 |
| GFX_RX13P | R6 |
| GFX_RX14N | P3 |
| GFX_RX14P | P4 |
| GFX_RX15N | T3 |
| GFX_RX15P | T4 |
| GFX_RX1N | B3 |
| GFX_RX1P | A3 |
| GFX_RX2N | C1 |
| GFX_RX2P | C2 |
| GFX_RX3N | F5 |
| GFX_RX3P | E5 |
| GFX_RX4N | G6 |
| GFX_RX4P | G5 |
| GFX_RX5N | H6 |
| GFX_RX5P | H5 |
| GFX_RX6N | J5 |
| GFX_RX6P | J6 |
| GFX_RX7N | J8 |
| GFX_RX7P | J7 |
| GFX_RX8N | L6 |
| GFX_RX8P | L5 |
| GFX_RX9N | L8 |
| GFX_RX9P | M8 |
| GFX_TX0N | B5 |
| GFX_TX0P | A5 |
| GFX_TX10N | K3 |
| GFX_TX10P | K4 |
| GFX_TX11N | K2 |
| GFX_TX11P | K1 |
| GFX_TX12N | M3 |
| GFX_TX12P | M4 |
| GFX_TX13N | M2 |
| GFX_TX13P | M1 |
| GFX_TX14N | N1 |
| GFX_TX14P | N2 |
| GFX_TX15N | P2 |
| GFX_TX15P | P1 |
| GFX_TX1N | B4 |
| GFX_TX1P | A4 |
| GFX_TX2N | B2 |
| GFX_TX2P | C3 |
| GFX_TX3N | D2 |
| GFX_TX3P | D1 |
| GFX_TX4N | E1 |
| GFX_TX4P | E2 |
| GFX_TX5N | F3 |
| GFX_TX5P | F4 |
| GFX_TX6N | F2 |
| GFX_TX6P | F1 |
| GFX_TX7N | H3 |
| GFX_TX7P | H4 |
| GFX_TX8N | H2 |
| GFX_TX8P | H1 |
| GFX_TX9N | J1 |
| GFX_TX9P | J2 |
| GPIO2 | F7 |
| GPIO3 | E9 |
| GPIO4 | G12 |
| GPP_REFCLKN | U2 |
| GPP_REFCLKP | U1 |
| GPP_RX0N | AD4 |
| GPP_RX0P | AE3 |
| GPP_RX1N | AD3 |
| GPP_RX1P | AE2 |
| GPP_RX2N | AD2 |
| GPP_RX2P | AD1 |
| GPP_RX3N | W6 |
| GPP_RX3P | V5 |
| GPP_RX4N | U6 |
| GPP_RX4P | U5 |
| GPP_RX5N | U7 |
| GPP_RX5P | U8 |
| GPP_TX0N | AC2 |
| GPP_TX0P | AC1 |
| GPP_TX1N | AB3 |
| GPP_TX1P | AB4 |
| GPP_TX2N | AA1 |
| GPP_TX2P | AA2 |
| GPP_TX3N | Y2 |
| GPP_TX3P | Y1 |
| GPP_TX4N | Y3 |
| GPP_TX4P | Y4 |
| GPP_TX5N | V2 |
| GPP_TX5P | V1 |
| GPPSB_REFCLKN | V3 |
| GPPSB_REFCLKP | V4 |
| HT_REFCLKN | C24 |
| HT_REFCLKP | C25 |
| HT_RXCAD0N | Y24 |
| HT_RXCAD0P | Y25 |
| HT_RXCAD10N | AA25 |
| HT_RXCAD10P | AA24 |
| HT_RXCAD11N | Y23 |
| HT_RXCAD11P | Y22 |
| HT_RXCAD12N | W20 |
| HT_RXCAD12P | W21 |
| HT_RXCAD13N | V20 |
| HT_RXCAD13P | V21 |
| HT_RXCAD14N | U21 |
| HT_RXCAD14P | U20 |
| HT_RXCAD15N | U18 |
| HT_RXCAD15P | U19 |
| HT_RXCAD1N | V23 |
| HT_RXCAD1P | V22 |
| HT_RXCAD2N | V24 |

| Pin Name | Ball Ref |
|---|---|
| HT_RXCAD2P | V25 |
| HT_RXCAD3N | U25 |
| HT_RXCAD3P | U24 |
| HT_RXCAD4N | T24 |
| HT_RXCAD4P | T25 |
| HT_RXCAD5N | P23 |
| HT_RXCAD5P | P22 |
| HT_RXCAD6N | P24 |
| HT_RXCAD6P | P25 |
| HT_RXCAD7N | N25 |
| HT_RXCAD7P | N24 |
| HT_RXCAD8N | AC25 |
| HT_RXCAD8P | AC24 |
| HT_RXCAD9N | AB24 |
| HT_RXCAD9P | AB25 |
| HT_RXCALN | A24 |
| HT_RXCALP | C23 |
| HT_RXCLK0N | T23 |
| HT_RXCLK0P | T22 |
| HT_RXCLK1N | AA22 |
| HT_RXCLK1P | AB23 |
| HT_RXCTL0N | M23 |
| HT_RXCTL0P | M22 |
| HT_RXCTL1N | R20 |
| HT_RXCTL1P | R21 |
| HT_TXCAD0N | D25 |
| HT_TXCAD0P | D24 |
| HT_TXCAD10N | J21 |
| HT_TXCAD10P | J20 |
| HT_TXCAD11N | K17 |
| HT_TXCAD11P | J18 |
| HT_TXCAD12N | J19 |
| HT_TXCAD12P | L19 |
| HT_TXCAD13N | L18 |
| HT_TXCAD13P | M19 |
| HT_TXCAD14N | P21 |
| HT_TXCAD14P | M21 |
| HT_TXCAD15N | M18 |
| HT_TXCAD15P | P18 |
| HT_TXCAD1N | E25 |
| HT_TXCAD1P | E24 |
| HT_TXCAD2N | F25 |
| HT_TXCAD2P | F24 |
| HT_TXCAD3N | F22 |

| Pin Name | Ball Ref |
|---|---|
| HT_TXCAD3P | F23 |
| HT_TXCAD4N | H22 |
| HT_TXCAD4P | H23 |
| HT_TXCAD5N | J24 |
| HT_TXCAD5P | J25 |
| HT_TXCAD6N | K25 |
| HT_TXCAD6P | K24 |
| HT_TXCAD7N | K22 |
| HT_TXCAD7P | K23 |
| HT_TXCAD8N | G21 |
| HT_TXCAD8P | F21 |
| HT_TXCAD9N | H21 |
| HT_TXCAD9P | G20 |
| HT_TXCALN | B25 |
| HT_TXCALP | B24 |
| HT_TXCLK0N | H25 |
| HT_TXCLK0P | H24 |
| HT_TXCLK1N | L20 |
| HT_TXCLK1P | L21 |
| HT_TXCTL0N | M25 |
| HT_TXCTL0P | M24 |
| HT_TXCTL1N | R18 |
| HT_TXCTL1P | P19 |
| IOPLLVDD | AE24 |
| IOPLLVDD18 | AE23 |
| IOPLLVSS | AD23 |
| LDTSTOP# | C10 |
| MEM_VREF | AE18 |
| NC | A16 |
| NC | A17 |
| NC | A18 |
| NC | A19 |
| NC | A20 |
| NC | A21 |
| NC | A22 |
| NC | A7 |
| NC | A8 |
| NC | A9 |
| NC | AA12 |
| NC | AA15 |
| NC | AA17 |
| NC | AA18 |
| NC | AA19 |
| NC | AA20 |

| Pin Name | Ball Ref |
|---|---|
| NC | AB12 |
| NC | AB13 |
| NC | AB14 |
| NC | AB16 |
| NC | AB18 |
| NC | AB20 |
| NC | AC14 |
| NC | AC16 |
| NC | AC18 |
| NC | AC20 |
| NC | AC22 |
| NC | AD12 |
| NC | AD13 |
| NC | AD14 |
| NC | AD15 |
| NC | AD16 |
| NC | AD17 |
| NC | AD18 |
| NC | AD19 |
| NC | AD20 |
| NC | AD21 |
| NC | AD22 |
| NC | AE12 |
| NC | AE13 |
| NC | AE15 |
| NC | AE16 |
| NC | AE17 |
| NC | AE19 |
| NC | AE21 |
| NC | AE22 |
| NC | B16 |
| NC | B17 |
| NC | B18 |
| NC | B19 |
| NC | B20 |
| NC | B21 |
| NC | B22 |
| NC | B7 |
| NC | B8 |
| NC | B9 |
| NC | C8 |
| NC | D10 |
| NC | D16 |
| NC | D17 |

| Pin Name | Ball Ref |
|---|---|
| NC | D18 |
| NC | D19 |
| NC | D20 |
| NC | D21 |
| NC | D9 |
| NC | E17 |
| NC | E18 |
| NC | E19 |
| NC | E8 |
| NC | F15 |
| NC | F17 |
| NC | F8 |
| NC | G14 |
| NC | G18 |
| NC | V11 |
| NC | V14 |
| NC | V15 |
| NC | V17 |
| NC | W12 |
| NC | W14 |
| NC | W17 |
| NC | W18 |
| NC | Y12 |
| NC | Y14 |
| NC | Y15 |
| NC | Y17 |
| NC | Y19 |
| PCE_CALRN | AB8 |
| PCE_CALRP | AC8 |
| PLLVDD | A12 |
| PLLVDD18 | D14 |
| PLLVSS | B12 |
| POWERGOOD | A10 |
| REFCLK_N | F11 |
| REFCLK_P | E11 |
| RESERVED | G11 |
| SB_RX0N | Y8 |
| SB_RX0P | AA8 |
| SB_RX1N | Y7 |
| SB_RX1P | AA7 |
| SB_RX2N | AA6 |
| SB_RX2P | AA5 |
| SB_RX3N | Y5 |
| SB_RX3P | W5 |

| Pin Name | Ball Ref |
|---|---|
| SB_TX0N | AE7 |
| SB_TX0P | AD7 |
| SB_TX1N | AD6 |
| SB_TX1P | AE6 |
| SB_TX2N | AC6 |
| SB_TX2P | AB6 |
| SB_TX3N | AE5 |
| SB_TX3P | AD5 |
| STRP_DATA | B10 |
| SUS_STAT# | D12 |
| SYSRESET# | D8 |
| TESTMODE | D13 |
| THERMALDIODE_N | AD8 |
| THERMALDIODE_P | AE8 |
| VDD_MEM | AA11 |
| VDD_MEM | AB10 |
| VDD_MEM | AC10 |
| VDD_MEM | AD10 |
| VDD_MEM | AE10 |
| VDD_MEM | Y11 |
| VDD18 | F9 |
| VDD18 | G9 |
| VDD18_MEM | AD11 |
| VDD18_MEM | AE11 |
| VDD33 | H11 |
| VDD33 | H12 |
| VDDA18HTPLL | H17 |
| VDDA18PCIE | AA9 |
| VDDA18PCIE | AB9 |
| VDDA18PCIE | AD9 |
| VDDA18PCIE | AE9 |
| VDDA18PCIE | H9 |
| VDDA18PCIE | J10 |
| VDDA18PCIE | K10 |
| VDDA18PCIE | L10 |
| VDDA18PCIE | M10 |
| VDDA18PCIE | P10 |
| VDDA18PCIE | R10 |
| VDDA18PCIE | T10 |
| VDDA18PCIE | U10 |
| VDDA18PCIE | W9 |
| VDDA18PCIE | Y9 |
| VDDA18PCIEPLL | D7 |
| VDDA18PCIEPLL | E7 |

| Pin Name | Ball Ref |
|---|---|
| VDDC | J11 |
| VDDC | J14 |
| VDDC | J16 |
| VDDC | K12 |
| VDDC | K15 |
| VDDC | L11 |
| VDDC | L14 |
| VDDC | M12 |
| VDDC | M13 |
| VDDC | M15 |
| VDDC | N12 |
| VDDC | N14 |
| VDDC | P11 |
| VDDC | P13 |
| VDDC | P14 |
| VDDC | R12 |
| VDDC | R15 |
| VDDC | T11 |
| VDDC | T14 |
| VDDC | T15 |
| VDDC | U12 |
| VDDC | U16 |
| VDDHT | J17 |
| VDDHT | K16 |
| VDDHT | L16 |
| VDDHT | M16 |
| VDDHT | P16 |
| VDDHT | R16 |
| VDDHT | T16 |
| VDDHTRX | A23 |
| VDDHTRX | B23 |
| VDDHTRX | D22 |
| VDDHTRX | E21 |
| VDDHTRX | F20 |
| VDDHTRX | G19 |
| VDDHTRX | H18 |
| VDDHTTX | AA21 |
| VDDHTTX | AB22 |
| VDDHTTX | AC23 |
| VDDHTTX | AD24 |
| VDDHTTX | AE25 |
| VDDHTTX | M17 |
| VDDHTTX | P17 |
| VDDHTTX | R17 |

| Pin Name | Ball Ref |
|---|---|
| VDDHTTX | T17 |
| VDDHTTX | U17 |
| VDDHTTX | V18 |
| VDDHTTX | W19 |
| VDDHTTX | Y20 |
| VDDLT18 | A15 |
| VDDLT18 | B15 |
| VDDLT33 | A14 |
| VDDLT33 | B14 |
| VDDLTP18 | A13 |
| VDDPCIE | A6 |
| VDDPCIE | B6 |
| VDDPCIE | C6 |
| VDDPCIE | D6 |
| VDDPCIE | E6 |
| VDDPCIE | F6 |
| VDDPCIE | G7 |
| VDDPCIE | H8 |
| VDDPCIE | J9 |
| VDDPCIE | K9 |
| VDDPCIE | L9 |
| VDDPCIE | M9 |
| VDDPCIE | P9 |
| VDDPCIE | R9 |
| VDDPCIE | T9 |
| VDDPCIE | U9 |
| VDDPCIE | V9 |
| VSS | AA14 |
| VSS | AB11 |
| VSS | AB15 |
| VSS | AB17 |
| VSS | AB19 |
| VSS | AB21 |
| VSS | AC12 |
| VSS | AE14 |
| VSS | AE20 |
| VSS | D11 |
| VSS | E14 |
| VSS | E15 |
| VSS | F18 |
| VSS | F19 |
| VSS | G17 |
| VSS | G8 |
| VSS | J12 |

| Pin Name | Ball Ref |
|---|---|
| VSS | J15 |
| VSS | K11 |
| VSS | K14 |
| VSS | L12 |
| VSS | L15 |
| VSS | M11 |
| VSS | M14 |
| VSS | N13 |
| VSS | P12 |
| VSS | P15 |
| VSS | R11 |
| VSS | R14 |
| VSS | T12 |
| VSS | U11 |
| VSS | U14 |
| VSS | U15 |
| VSS | V12 |
| VSS | W11 |
| VSS | W15 |
| VSS | Y18 |
| VSSAHT | A25 |
| VSSAHT | AD25 |
| VSSAHT | D23 |
| VSSAHT | E22 |
| VSSAHT | G22 |
| VSSAHT | G24 |
| VSSAHT | G25 |
| VSSAHT | H19 |
| VSSAHT | H20 |
| VSSAHT | J22 |
| VSSAHT | L17 |
| VSSAHT | L22 |
| VSSAHT | L24 |
| VSSAHT | L25 |
| VSSAHT | M20 |
| VSSAHT | N22 |
| VSSAHT | P20 |
| VSSAHT | R19 |
| VSSAHT | R22 |
| VSSAHT | R24 |
| VSSAHT | R25 |
| VSSAHT | U22 |
| VSSAHT | V19 |
| VSSAHT | W22 |

| Pin Name | Ball Ref |
|---|---|
| VSSAHT | W24 |
| VSSAHT | W25 |
| VSSAHT | Y21 |
| VSSAPCIE | A2 |
| VSSAPCIE | AA4 |
| VSSAPCIE | AB1 |
| VSSAPCIE | AB2 |
| VSSAPCIE | AB5 |
| VSSAPCIE | AB7 |
| VSSAPCIE | AC3 |
| VSSAPCIE | AC4 |
| VSSAPCIE | AE1 |
| VSSAPCIE | AE4 |
| VSSAPCIE | B1 |
| VSSAPCIE | D3 |
| VSSAPCIE | D5 |
| VSSAPCIE | E4 |
| VSSAPCIE | G1 |
| VSSAPCIE | G2 |
| VSSAPCIE | G4 |
| VSSAPCIE | H7 |
| VSSAPCIE | J4 |
| VSSAPCIE | L1 |
| VSSAPCIE | L2 |
| VSSAPCIE | L4 |
| VSSAPCIE | L7 |
| VSSAPCIE | M6 |
| VSSAPCIE | N4 |
| VSSAPCIE | P6 |
| VSSAPCIE | R1 |
| VSSAPCIE | R2 |
| VSSAPCIE | R4 |
| VSSAPCIE | R7 |
| VSSAPCIE | U4 |
| VSSAPCIE | V6 |
| VSSAPCIE | V7 |
| VSSAPCIE | V8 |
| VSSAPCIE | W1 |
| VSSAPCIE | W2 |
| VSSAPCIE | W4 |
| VSSAPCIE | W7 |
| VSSAPCIE | W8 |
| VSSAPCIE | Y6 |
| VSSLT | C14 |

| Pin Name | Ball Ref |
|---|---|
| VSSLT | C16 |
| VSSLT | C18 |
| VSSLT | C20 |
| VSSLT | C22 |
| VSSLT | D15 |
| VSSLT | E20 |
| VSSLTP18 | B13 |

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# Appendix B
## *Revision History*

**Rev. 1.30 (Nov 2010)**

- First release of the public version.

**Rev. 1.40 (Aug 2011)**

- Updated Figure 1-1, “RX881 ASIC A11 Production Branding.”

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